Memory System Design
with the Intel® 2107B
4K RAM

Jim Oliphant
Application Engineering

©Intel Corporation, 1975
TOPOGRAPHY OF THE 2107B
# Memory System Design with the Intel® 2107B 4K RAM

## Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>INTERNAL DEVICE OPERATION</td>
<td>1</td>
</tr>
<tr>
<td>Storage Cell Operation</td>
<td>2</td>
</tr>
<tr>
<td>Data Sense/Latch</td>
<td>3</td>
</tr>
<tr>
<td>Address Buffer/Latch</td>
<td>3</td>
</tr>
<tr>
<td>Output Driver</td>
<td>4</td>
</tr>
<tr>
<td>2107B Bit Map</td>
<td>4</td>
</tr>
<tr>
<td>2107B SPECIFICATION</td>
<td>4</td>
</tr>
<tr>
<td>Timing</td>
<td>6</td>
</tr>
<tr>
<td>Transient Currents</td>
<td>6</td>
</tr>
<tr>
<td>SYSTEM CONSIDERATIONS</td>
<td>9</td>
</tr>
<tr>
<td>MOS Level Drivers</td>
<td>9</td>
</tr>
<tr>
<td>3235 MOS Level Driver</td>
<td>10</td>
</tr>
<tr>
<td>3210 MOS Level Driver</td>
<td>12</td>
</tr>
<tr>
<td>Low Voltage Driver/Buffers</td>
<td>13</td>
</tr>
<tr>
<td>TTL Drivers</td>
<td>14</td>
</tr>
<tr>
<td>Other Low Voltage Driver/Buffers</td>
<td>16</td>
</tr>
<tr>
<td>Output Sensing</td>
<td>17</td>
</tr>
<tr>
<td>System Timing and Control</td>
<td>17</td>
</tr>
<tr>
<td>Memory Array Layout</td>
<td>21</td>
</tr>
<tr>
<td>Decoupling</td>
<td>22</td>
</tr>
<tr>
<td>Debugging A Memory System</td>
<td>23</td>
</tr>
<tr>
<td>Power Calculations</td>
<td>25</td>
</tr>
<tr>
<td>Device Power</td>
<td>25</td>
</tr>
<tr>
<td>System Power</td>
<td>26</td>
</tr>
<tr>
<td>Power Supply Sequencing</td>
<td>26</td>
</tr>
<tr>
<td>ACKNOWLEDGMENT</td>
<td>26</td>
</tr>
<tr>
<td>2107B SPECIFICATIONS</td>
<td>27</td>
</tr>
<tr>
<td>2107B SELECTION GUIDE</td>
<td>Inside Back Cover</td>
</tr>
</tbody>
</table>

Intel Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in an Intel® product. No other circuit patent licenses are implied.
INTRODUCTION

The Intel® 2107B is a 4096 word by 1 bit dynamic random access memory. The 2107B is fabricated using Intel’s standard reliability proven n-channel silicon gate MOS technology. The device is packaged in a standard 22-pin DIP. The pin configuration and logic symbol are shown in Figure 1. Note that the 2107B can be used as a replacement for the 2107A.

LOGIC SYMBOL

PIN CONFIGURATION

The combination of Intel’s® n-channel silicon gate process and circuit design has resulted in a part that is very fast, easy to use, and economically produced in large volume. In addition, the combination of process and device design has resulted in a very small device (see Figure 2) using conservative layout rules (same as 2102A). The small size offers advantages in both large volume production and increased reliability. The 2107B operates with three power supplies relative to ground; \( V_{DD} (+12V) \), \( V_{BB} (-5V) \), and \( V_{CC} (+5V) \). The \( V_{CC} (+5V) \) supply is connected only to the output buffer of the 2107B and may be turned off during power down operations.

INTERNAL DEVICE OPERATION

The 2107B has one MOS level clock (Chip Enable) with all other inputs being low level TTL compatible (+2.4V \( V_{IH} \) minimum). The output is capable of driving 1 TTL load.

The purpose of this application note is to describe the internal operation of the 2107B, outline those areas in system implementation to which the designer should pay particular attention and to discuss typical examples of the uses of the 2107B in systems environment. The application note is arranged so that each of the above sections can be read independently of each other without having to go through any unwanted detail in the other sections.

The 2107B can be used as a replacement for the 2107A.

LOGIC SYMBOL

PIN CONFIGURATION

Figure 1. 2107B Logic Symbol and Pin Configuration

The 2107B has one MOS level clock (Chip Enable) with all other inputs being low level TTL compatible (+2.4V \( V_{IH} \) minimum). The output is capable of driving 1 TTL load.

The purpose of this application note is to describe the internal operation of the 2107B, outline those areas in system implementation to which the designer should pay particular attention and to discuss typical examples of the uses of the 2107B in systems environment. The application note is arranged so that each of the above sections can be read independently of each other without having to go through any unwanted detail in the other sections.

INTERNAL DEVICE OPERATION

Internal operation of the 2107B is most easily understood with the aid of the block diagram shown in Figure 3. As is shown in this figure, the memory array is arranged in a 64 row X 64 column matrix of storage cells. The storage cells are implemented with a single transistor and a “storage” capacitor and are called single transistor cells. The operation of the storage cell will be discussed later.

The memory cell is accessed by the coincidence of a row select (defined by addresses \( A_0 - A_8 \)) and a column select (defined by addresses \( A_6 - A_11 \)) signal at the desired address. An on chip timing and control generator provides for the internal timing signals for decoding, read/write strobing, data gating and output gating. All of the timing circuits in the 2107B are activated by the positive-going edge of chip enable.

Chip select controls the data I/O gating circuits internal to the 2107B. When chip select is high the output data buffer is in a high impedance state and

BLOCK DIAGRAM

Figure 2. 2107B Comparative Die Size

Figure 3. 2107B Block Diagram
the data-in buffer is electrically isolated from the data-in input pin. Since chip select controls only the internal data buffers and not the timing generators or address buffers internal to the 2107B, it is possible to refresh the 2107B with chip select high by initiating a read/refresh or write cycle.

The address buffer registers consist of latches activated at the leading edge of chip enable. Since the addresses are latched shortly after chip enable goes high, it is permissible to change the address long before the memory cycle is completed to set up for the next cycle.

The write enable input activates the data-in buffer gating data to the selected memory cell. Input data must be valid at the time write enable goes low to assure that the proper data is written into memory.

Circuit implementation and operation of each of the major input/output and storage portions are discussed below.

Storage Cell Operation

The storage cell used in the 2107B is implemented with a single transistor and storage capacitor as shown in Figure 4. From this figure it is shown that a charge on a storage cell is gated to the bit sense line by the MOS device connected to the column select line. (Note that for a given column select, 64 storage devices are gated to the respective 64 bit sense lines.)

Consider first a read operation and the case where the storage capacitor \( C_{STG} \) is discharged; i.e., node 1 is at \( V_{SS} \) (GND). Prior to chip enable going high, the bit sense lines have been precharged to \( V' \) by device \( Q_1 \). [\( V' \) is a voltage between \( V_{DD} (12V) \) and \( V_{SS} \).] After the address decoders have stabilized, the proper column select line is brought high, turning on device \( Q_2 \). The storage capacitor is then electrically connected to the bit sense line. At this time the charge on \( C_{I/O} \) (proportional to the pre-charge voltage \( V' \)) is redistributed between \( C_{I/O} \) (parasitic capacitance of bit sense line) and \( C_{STG} \). Since \( C_{STG} \) was initially discharged (node 1 at \( V_{SS} \)) the voltage will distribute between \( C_{I/O} \) and \( C_{STG} \) according to the following relationship:

\[
V_{BIT \ SENSE} (t_1) = V_{BIT \ SENSE} (t_0) \left( \frac{C_{I/O}}{C_{I/O} + C_{STG}} \right)
\]

Since \( C_{I/O} \) is very much larger than \( C_{STG} \) the change in the voltage on the bit sense line will be very small. The sense amplifier (S/A) is designed to detect very small changes in bit sense line voltage and to latch in a state near \( V_{SS} \) (GND) or \( V_{DD} (+12V) \), depending on the state of the storage cell.

Sensing an initial charge on \( C_{STG} \) (proportional to \( V_x \) where \( V_x = V_{DD}-V_{TH} \), \( V_{TH} \) is the effective MOS threshold) is identical to the sequence described above. The only difference is that now the bit sense line is driven above the initial \( V' \) precharge voltage. Again the sense amplifier detects the small change in bit sense line voltage and latches in the appropriate state.

Note that during a read operation of the storage cell, the original charge (data) on the storage cell is changed (i.e., the read operation is effectively a destructive read). Data is rewritten back on the storage capacitor \( C_{STG} \) by the sense amplifier after it has latched in the proper state. For example, if \( C_{STG} \) was initially charged to \( V_x \) (~10V), the sense amplifier will latch the bit sense line to \( V_x \) and, since the column select line is on (high), the original data is automatically rewritten into \( C_{STG} \). The entire operation is transparent to the user.

A plot of the voltage on the bit sense line for the two cases described above is shown in Figure 5.
A write operation is identical to the rewrite portion of a read cycle. In this case, however, the incoming data "overrides" the state of the sense amplifier (if different from the desired state) and writes into the selected cell. For reference, a low level on the data-in input results in a high level (Vx) being written into the selected storage cell. It is important to remember that the data-output at the output pin is the logical inverse of the data written into memory.

Data Sense/Latch

As discussed previously, a sense amplifier on the bit sense line is necessary to detect the low level data signals generated on the bit sense line during a read cycle. A simplified circuit schematic used for the sense amplifier is shown in Figure 6.

Before chip enable is brought high, both sides of the bit sense lines are precharged to V' (as discussed previously). At the proper time (after all data transients have subsided) devices Q1 and Q2 are turned on by φR going positive. At this time, the state of bit sense left is compared with bit sense right causing the latch to lock in the appropriate state. For example, if the right bit sense line is at a higher potential than the left bit sense line, device Q3 will begin to conduct. The cross coupled latch will then fully switch with bit sense left going to VSS and bit sense right to VX.

Address Buffer/Latch

The address buffer/latch is shown in Figure 7. The input to the address buffer/latch is low voltage compatible which the circuit senses, translates to MOS level signals and latches.

Operation of the address buffers is as follows: During chip enable off time (CE low) both sides of the latch are precharged to VX (~10V) by devices Q1, Q2, and Q3. Device Q3 is used to assure that the initial precharge on each side of the latch are equal.

When chip enable goes high, the input to the address buffer (AIN) is gated to the cross coupled latch which latches the appropriate MOS level at A1 and A1. For example, if the TTL address input is high, then device Q7 will turn on at φA time. The cross coupled latch then regenerates, turning Q6 off. The quiescent state of the latch for this input is Q6 off, Q8 on, thereby setting A1 and A1 to MOS level high and low, respectively.

This type of latch is capable of triggering and latching at very high speeds which allows the addresses to be removed from the input as soon as possible. However, there are a few characteristics of this latch which have an effect when the device is placed in a system environment.

First note that node (1), Figure 7, has been precharged to a high MOS level of VX (~10V). When
chip enable goes high turning on Q4, the charge on this node is connected to the address input node (AIN) for a short period of time (until the latch switches). This results in a small positive voltage shift on the address input AIN. It follows then that the more 2107B devices attached to a given address driver the larger the voltage excursion will be. This excursion has been found to cause no problem in any reasonable system environment (as described later) and amounts to no more than 9 mV positive shift for each 2107B. The amount of positive charge coupling depends upon the address driver and the address line impedance. As should be expected, the most sensitive address level is the low level (VIL) since any positive coupling decreases the available noise margin.

Another characteristic to be aware of in this type address buffer is the input current drawn through the address driver when an address goes from a low state to a high state during chip enable high. This condition results from the latch being set in the state where Q6 is on as well as Q4 and Q5. Current is then drawn through devices Q4, Q5, Q6 and Q9. This current is typically in the order of 0.5 mA. Note that although this may cause a load on the address driver and cause it to drop below 2.4V, there is no effect on the memory component since the desired address has been latched in. This current is drawn only as long as chip enable is high. When chip enable goes low, device Q4 is turned off, opening the current path. This effect will be shown on various type drivers in a later section (Low Voltage Buffer/Drivers).

Output Driver

A schematic of the output buffer is shown in Figure 8. Note that the output is in a high impedance state if either chip select is high or chip enable is low. Further, the VCC shown in Figure 8 is the only connection the VCC makes on the 2107B. This allows VCC to have a wide range of values (up to VDD) if types of sensing other than TTL is desired.

2107B Bit Map

Figure 9 gives the location of each cell in the memory matrix for each address. As shown in this figure, the addresses run sequentially starting from the lower left corner (device oriented as shown).

2107B SPECIFICATION

Although the device specifications for the 2107B are concise and self explanatory, some sections are included here to emphasize those areas of most interest to the designer. Consider first the DC and operating characteristics shown in Table I marked with a [5].

The VDD supply current during chip enable off is specified at 200 µA maximum with chip enable no higher than 0.6V. It is important to hold the low level of chip enable at or below this value (to a maximum of -1.0V) to assure that devices internal to the 2107B do not turn partially on. Note that considering only the AC operating environment, chip enable can go as high as 1.0V above VSS and the device will still operate properly. This requirement on chip enable off is most important in those systems being placed in a low power refresh only standby mode.

The VBB supply current load (IBB) is maximum at 100 µA and includes all leakages. It is not necessary to add the other leakage currents (e.g., ILI, ILC) to IBB to calculate supply drain on VBB.

The input low voltage (for low level signals) VIL, is specified as a function of the chip enable rise time and is referenced to a transition with tT = 20 nsec. It is recognized that in some system applications, the load on the chip enable driver may result in transitions of 30 nsec or higher (to a maximum of 40 nsec). If the chip enable transition in the system is not 20 nsec or faster (to a minimum of 10 nsec), then the typical low level for the low level drivers is shown by the graph in Figure 10. It is important to include any noise which may be on the address line during tAH (address hold) time. An example of the noise expected on an address line when chip enable goes high (during refresh) is shown in Figure 11. The noise shown here is the result of 36 devices attempting to raise the address driver (see Address Buffer/Latch) level during refresh time. Refresh
Table I. D.C. and Operating Characteristics

\( T_A = 0^\circ C \) to \( 70^\circ C \), \( V_{DD} = +12V \pm 5% \), \( V_{CC} = +5V \pm 5% \), \( V_{BB} \text{[1]} = -5V \pm 5% \), \( V_{SS} = 0V \), unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN.</th>
<th>TYP. \text{[2]}</th>
<th>MAX.</th>
<th>UNIT</th>
<th>CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{IL} )</td>
<td>Input Load Current (All Inputs Except CE)</td>
<td>.01</td>
<td>10</td>
<td>( \mu A )</td>
<td>( V_{IN} = V_{IL} \text{ MIN} ) to ( V_{IH} \text{ MAX} )</td>
<td></td>
</tr>
<tr>
<td>( I_{IC} )</td>
<td>Input Load Current</td>
<td>.01</td>
<td>10</td>
<td>( \mu A )</td>
<td>( V_{IN} = V_{IL} \text{ MIN} ) to ( V_{IH} \text{ MAX} )</td>
<td></td>
</tr>
<tr>
<td>( I_{ILO} )</td>
<td>Output Leakage Current for High Impedance State</td>
<td>.01</td>
<td>10</td>
<td>( \mu A )</td>
<td>( CE = V_{ILC} \text{ or } CS = V_{IH} )  ( V_O = 0V ) to ( 5.25V )</td>
<td></td>
</tr>
<tr>
<td>( I_{DD1} \text{[5]} )</td>
<td>( V_{DD} ) Supply Current During CE Off</td>
<td>110</td>
<td>200</td>
<td>( \mu A )</td>
<td>( CE = -1V ) to ( +0.6V )</td>
<td></td>
</tr>
<tr>
<td>( I_{DD2} )</td>
<td>( V_{DD} ) Supply Current During CE On</td>
<td>80</td>
<td>100</td>
<td>mA</td>
<td>( CE = V_{IH} )  ( T_A = 25^\circ C )</td>
<td></td>
</tr>
<tr>
<td>( I_{DD AV1} )</td>
<td>Average ( V_{DD} ) Current</td>
<td>55</td>
<td>80</td>
<td>mA</td>
<td>Cycle Time = ( 400 ns ), ( t_{CE} = 230 ns )  ( T_A = 25^\circ C )</td>
<td></td>
</tr>
<tr>
<td>( I_{DD AV2} )</td>
<td>Average ( V_{DD} ) Current</td>
<td>27</td>
<td>40</td>
<td>mA</td>
<td>Cycle Time = ( 1000 ns ), ( t_{CE} = 230 ns )  ( T_A = 25^\circ C )</td>
<td></td>
</tr>
<tr>
<td>( I_{CC1} \text{[4]} )</td>
<td>( V_{CC} ) Supply Current During CE Off</td>
<td>.01</td>
<td>10</td>
<td>( \mu A )</td>
<td>( CE = V_{ILC} \text{ or } CS = V_{IH} )</td>
<td></td>
</tr>
<tr>
<td>( I_{BB} \text{[5]} )</td>
<td>( V_{BB} ) Supply Current</td>
<td>5</td>
<td>100</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IL} \text{[5]} )</td>
<td>Input Low Voltage</td>
<td>(-1.0 )</td>
<td>( 0.6 )</td>
<td>V</td>
<td>( t_T = 20 ns ) – See Figure 4</td>
<td></td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input High Voltage</td>
<td>2.4</td>
<td>( V_{CC} \text{+1} )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{ILC} )</td>
<td>CE Input Low Voltage</td>
<td>(-1.0 )</td>
<td>(+1.0 )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{IHC} \text{[5]} )</td>
<td>CE Input High Voltage</td>
<td>( V_{DD} \text{-1} )</td>
<td>( V_{DD} \text{+1} )</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Low Voltage</td>
<td>0.0</td>
<td>0.45</td>
<td>V</td>
<td>( I_{OL} = 2.0 \text{ mA} )</td>
<td></td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>( V_{CC} )</td>
<td>V</td>
<td>( I_{OH} = -2.0 \text{ mA} )</td>
<td></td>
</tr>
</tbody>
</table>

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that \( V_{DD} \), \( V_{CC} \), and \( V_{SS} \) should never be \( 0.3V \) more negative than \( V_{BB} \).
2. Typical values are for \( T_A = 25^\circ C \) and nominal power supply voltages.
3. The \( I_{DD} \) and \( I_{CC} \) currents flow to \( V_{SS} \). The \( I_{BB} \) current is the sum of all leakage currents.
4. During CE on \( V_{CC} \) supply current is dependent on output loading, \( V_{CC} \) is connected to output buffer only.
5. See basic discussion – 2107B specifications.

Figure 10. \( V_{IL} \) vs CE Rise Time

Figure 11. Coupling to Address Line Caused by Chip Enable Transition
is the worst case since all chip enable signals will be simultaneously decoded and driven at the same time.

The chip enable high voltage, \( V_{IHC} \), can vary between \( V_{DD} + 1.0 \) and \( V_{DD} - 1.0 \) volts. This allows maximum flexibility in the driver design and provides for adequate noise margins.

The average \( V_{DD} \) current \( I_{DDAV1} \) during a read/write cycle is specified at 25°C to be a maximum of 80 ma. This current is a function of both cycle time and temperature as shown in Figures 12 and 13, respectively. As shown by these curves, the maximum power occurs at low temperature and maximum duty cycle.

**Transistor Currents**

Although the transistor currents in the 2107B are easily handled, proper attention should be paid to the peak values and adequate decoupling provided to handle the expected transients. Figure 17 shows the transient currents present in the 2107B.

Consider first the transient current supplied by the chip enable driver \( I_{CE} \). It is noted that this current does not have a resistive component but is strictly a charging current represented by the relationship:

\[
I = C \left( \frac{dv}{dt} \right)
\]

As expected, the largest transient current drawn by the 2107B is the \( V_{DD} \) supply and is represented by \( I_{PP} \). The first portion of this curve (peak ~120 ma) shown as A is the result of internal nodes charging up for operation. The section shown as B is the result of the address buffers/decoders turning off. Portion C is the “steady state” current drawn by all internal circuits while chip enable is high. Note the slight difference between a read and write cycle which results from different portions of the internal circuitry turning on.

Portion D of the transient current is the result of feedthrough capacitance (internal to the chip) coupling to \( V_{DD} \) when chip enable goes low. Portion E is the precharging of selected internal nodes by the chip enable generator (e.g., precharging bit sense line. See section on Internal Device Operation).

The transients associated with the \( V_{BB} \) supply \( I_{BB} \) should be reviewed closely. Note that the peak values are approximately 20 ma during a cycle with a time base as shown. Special attention is called to this because even though the average DC current is very small (maximum 100 \( \mu \)a) the peak currents can be two orders of magnitude higher.
(Numbers in parentheses are for minimum cycle timing in ns)

Figure 14. Read/Refresh Cycle

Figure 15. Write Cycle

NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{IL} MAX is the reference level for measuring timing of the addresses, CS, WE, and D_{IN}.
3. V_{IH} MIN is the reference level for measuring timing of the addresses, CS, WE, and D_{IN}.
4. V_{SS} +2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} +2.0V is the reference level for measuring the timing of D_{OUT}.
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.
NOTES:
1. A.C. characteristics are guaranteed only if cumulative CE on time during tREF is < 60% of tREF. For continuous Read-Modify-Write operation tCC and tRWC should be increased to at least 195ns and 585 ns, respectively.
2. VIL MAX is the reference level for measuring timing of the addresses, CS, WE, and DI.
3. VIH MIN is the reference level for measuring timing of the addresses, CS, WE, and DI.
4. VDD +2.0V is the reference level for measuring the timing of CE.
5. VSS -2V is the reference level for measuring the timing of CE.
6. VSS +2.0V is the reference level for measuring the timing of DOUT.
7. WE must be at VIH until end of tCO.
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.

Figure 16. Read-Modify-Write Cycle
These transients are characteristic of any dynamic RAM and are in part related to the density of the RAM. Again, if adequate decoupling measures are taken, very little noise will be generated on the VBB system distribution.

Notice that the transient current for ICC1 is not shown. This is because the VCC supply is connected only to the internal output device and its transient depends on the load placed on the output.

A full discussion on decoupling the power distribution in 2107B arrays appears in the decoupling section. As it is shown later, the use of a multi-layer memory board is not required by the 2107B.

SYSTEM CONSIDERATIONS

The previous sections of this application note have dealt with the characteristics of the 2107B as a stand-alone device. This section will outline the types of interface, system design considerations, power calculations and testing considerations when using the 2107B.

MOS Level Drivers

There are many types of drivers capable of driving n-channel RAMs such as the 2107B. The drivers can be used in one or more of the configurations as shown in Figure 18a, b, and c. Each of the driver types shown in Figure 18 has an optimum circuit load that it can drive and each has special design considerations. These drivers are categorized in three general types; those which:

1. Require external drive transistors.
2. Require an additional power supply.
3. Require no special components or voltages.

In case (1) above, there is insufficient high level drive capability in the driver, hence a PNP external discrete transistor must be used to generate sufficient up-going transition (Figure 18a). Note that this transistor is driving in the saturated mode so the minimum high level criteria (VDD=1.0) on the high level MOS clock are easily met.

Driver type (2), shown in Figure 18b, does not require external discrete transistors but does require an additional power supply. This extra supply is usually 3V higher than the VDD supply for the RAM (e.g., using this type of driver with the 2107B would require VDD = 12V and VDD1 = 15V). The additional supply is necessary to assure that the minimum up level (VDD-1.0) requirement of the MOS clock is met.

The high going drive capability of the driver type shown in Figure 18c may be insufficient to meet the VHI MIN requirements of the 2107B.

The types of MOS level drivers recommended to drive the 2107B (or any other n-channel MOS RAM) are those shown in Figure 18a and b.

![Figure 18. Three Types of MOS Level Drivers](image)

It is important to remember to place the MOS level driver outputs physically as close as possible to the memory array. This will minimize any transmission line impedance mismatch between the unloaded stub and heavily loaded line in the memory array. The effect can most easily be seen with the aid of Figure 19. The impedance of the interconnect is:

\[ Z_{0(1)} = \sqrt{\frac{L}{C_1}} \]

where \( C_1 \) is the capacitance per unit length of the interconnect

\( L \) is the inductance per unit length of the interconnect

![Figure 19. MOS Level Driver Loading](image)
For all practical purposes, the inductance per unit length of the printed line is independent of the externally connected loads. Therefore, the impedance of the loaded section of transmission line can be represented as:

\[ Z_0(2) = \sqrt{\frac{L}{C_1 + C_2}} \]

where \( C_2 \) is the added capacitance per unit length to the printed transmission line.

For most practical systems, capacitance per unit length of an unloaded transmission line will be approximately 1–2 pF/in. \( (C_1) \). \( C_2 \) is the capacitance effect of the 2107B per unit length. Since the spacing between memory devices is approximately 0.5" the typical loading effect of \( C_2 \) is 30 pF/in. \( (i.e., 15 \text{ pF assumed for each chip enable input).} \)

The ratio of the two impedances is calculated as follows:

\[ \frac{Z_0(1)}{Z_0(2)} = \sqrt{\frac{C_1+C_2}{C_1}} = \sqrt{\frac{32}{2}} = 4 \]

This means that the impedance of the stub is four times the impedance of the loaded section.

If the loads are placed close to the driver output the effect of the stub will be negligible and will cause no problem.

3235 MOS Level Driver

The Intel® 3235 is a quad MOS level driver, with each driver capable of driving 250 pF load with maximum delay of 32 nsec. The 3235 requires three power supplies \( V_{CC} (+5V) \), \( V_{DD1} (+12V) \), and \( V_{DD2} (+15V) \). The pin configuration and logic diagram of the 3235 is shown in Figure 20. For reference, input/output waveforms are shown in Figure 21, with delays given in Table II for worst case conditions.

Note that Table II gives the minimum input to output delay for a lightly loaded line \( (C = 150 \text{ pF}) \) and the maximum delay plus rise time for a heavier load \( (C = 250 \text{ pF}) \). The minimum delay time is given so the system designer can guarantee that the chip enable driven by a particular driver does not occur before the address lines have stabilized. The maximum delay plus rise time is given to guarantee

![Figure 20. 3235 Pin Configuration and Logic Diagram](image)

![Figure 21. 3235 Input/Output Waveforms](image)

Table II. 3235 A.C. Characteristics

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN.(^{[1]})</th>
<th>TYP.(^{[2]})</th>
<th>MAX.(^{[3]})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{+} )</td>
<td>Input to Output Delay</td>
<td>5</td>
<td>11</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{DR} )</td>
<td>Delay Plus Rise Time</td>
<td>20</td>
<td>32</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{+} )</td>
<td>Input to Output Delay</td>
<td>3</td>
<td>8</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>( t_{DF} )</td>
<td>Delay Plus Fall Time</td>
<td>19</td>
<td>32</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

\(^{[1]}\) \( C_L = 150 \text{ pF} \)

\(^{[2]}\) \( C_L = 200 \text{ pF} \)

\(^{[3]}\) \( T_A = 25^\circ C \)

\(^{[4]}\) \( C_L = 250 \text{ pF} \)

\(^{[5]}\) \( V_{CC} = 5.0V \pm 5\%, \ V_{DD1} = 12V \pm 5\%, \ V_{DD2} = V_{DD1} + (3V \pm 5\%) \)
a required system access or cycle time can be met. The capacitance values specified for the 3235 of 
$C = 150$ pF, $C = 200$ pF, and $C = 250$ pF are repre­
sentative of the minimum, typical, and maximum 
capacitance, respectively, of nine 2107B Chip En­
able inputs plus associated stray capacitance.

Graphs showing the effect of capacitance loads on 
delay and rise times are shown in Figure 22a and b.

![Figure 22. 3235 Delay and Transition Time as a Function of $C_{LOAD}$](image)

The 3235 offers a great deal of flexibility in driving 
large arrays of 2107Bs. A sample of its logic capa­
bility is shown in Figure 23. A given card is selected 
by Card Enable i, byte control is maintained with Byte Enable, and the desired row selected by Row 
Enable i. The basic chip enable timing pulse is provided by CE timing.

At refresh time it is necessary to activate the Card 
Enable i, Byte Enable and Refresh Enable to re­
fresh the entire card at one time. In most systems, 
it is desirable to refresh all cards simultaneously. If 
the cards are decoupled properly (see Decoupling section), the power supply transients during refresh 
will be minimal and are acceptable. The basic con­
figuration of such a card is shown in Figure 24. For 
this system, the entire 16K X 16 memory array can 
be driven with two 3235s placed as shown between 
the two memory arrays.

Waveforms of the 3235 driver in a system similar to 
that shown in Figure 24 are given in Figure 25a–d. 
The driver configuration used is shown in Figure 26. 
Figure 25a and b shows the leading and trailing edge 
of chip enable at both the beginning and ending of 
the printed line for an added series resistance $R$ of 
10Ω. Note the transition time and overshoot for 
each of these edges. The overshoot is worst case at 
the leading edge at the driver end and on the trail­
ing edge at the end of the line. The trailing edge 
overshoot is 2.2V while the leading edge overshoot 
is 1.5V. Both values are very marginal for system 
operation.

The effect of increasing the series resistance to 20Ω 
for the above driver is shown in Figure 24c and d. 
Note that the transition time has increased but is
still within entirely acceptable limits and the overshoots have been cut in half. The driver is now operating in an acceptable mode with minimal overshoot.

The effect of temperatures on the 3235 is shown in Figure 27. A 20Ω series resistor is used with the driver.

The results of board measurements of a typical 3235 driver driving 18 loads and 9 loads is shown in Table III. Note that the delay does not change appreciably with temperature but the transition time increased approximately 2–3 nsec from 25°C to 70°C.

Figure 25. 3235 Typical Driver Waveforms

Figure 26. MOS Level Driver Configuration

3210 MOS Level Driver
The pin configuration and logic symbol for the 3210 driver is shown in Figure 28. As shown in this figure, this driver consists of one MOS level driver and four TTL low voltage buffers. These low voltage buffers can be used to drive inputs which require a 3.5V high level (such as the 2107A address
Table III. Summary of 3235 Driver Board Delay Measurements

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>3235 18 LOADS[6] R = 20Ω</td>
<td>12</td>
<td>12</td>
<td>10</td>
</tr>
</tbody>
</table>

NOTES:
1. TTL 1.5 to VSS +1 volt
2. TTL 1.5 to VDD -1 volt
3. TTL 1.5 to VDD -1 volt
4. TTL 1.5 to VSS +1 volt
5. Worst case driver on board at 70°C and 5% power supply variation.
6. 18 loads 20Ω split resistor (see Figure 26).
7. Projected from 18 load delay.

Figure 28. 3210 Pin Configuration and Logic Symbol

inputs) or they can be used to drive high capacitance loads with minimum delay. For reference, the input/output characteristics of the 3210 are shown in Figure 29 and table IV, respectively.

The driver configuration for the 3210 MOS level output is shown with the aid of photos in Figure 30a and b for series resistances of 10Ω and 20Ω. Table V summarizes the results of board measurements for the 3210 as a function of series resistance and temperature.

Low Voltage Driver/Buffers

The address, data-in, write enable, and chip select inputs on the 2107B are all low voltage TTL compatible requiring no special interface. This section will discuss the types of drivers which can be used to drive the low voltage inputs along with the advantages and disadvantages of the drivers.

The types of low level drivers capable of driving the 2107B are shown in Figure 31. Two observations are pointed out regarding the use of TTL drivers shown in Figure 31.
1. There are no pull up resistors.
2. Series 74S type gates are not recommended.

Table IV. 3210 A.C. Characteristics

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>MIN.</th>
<th>TYP. [1]</th>
<th>MAX.</th>
<th>UNITS</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{LDR}</td>
<td>Delay Plus Rise Time for Low Voltage Drivers</td>
<td>17</td>
<td>25</td>
<td>nS</td>
<td>C_L = 200 pF</td>
<td></td>
</tr>
<tr>
<td>t_{LDP}</td>
<td>Delay Plus Fall Time for Low Voltage Drivers</td>
<td>16</td>
<td>25</td>
<td>nS</td>
<td>C_L = 200 pF</td>
<td></td>
</tr>
<tr>
<td>t_{H+ }</td>
<td>Input to Output Delay for High Voltage Driver</td>
<td>9</td>
<td>15</td>
<td>nS</td>
<td>C_L = 175 pF</td>
<td></td>
</tr>
<tr>
<td>t_{HDR}</td>
<td>Delay Plus Rise Time for High Voltage Driver</td>
<td>27</td>
<td>40</td>
<td>nS</td>
<td>C_L = 350 pF</td>
<td></td>
</tr>
<tr>
<td>t_{H- }</td>
<td>Input to Output Delay for High Voltage Driver</td>
<td>4</td>
<td>8</td>
<td>nS</td>
<td>C_L = 175 pF</td>
<td></td>
</tr>
<tr>
<td>t_{HDF}</td>
<td>Delay Plus Fall Time for High Voltage Driver</td>
<td>18</td>
<td>30</td>
<td>nS</td>
<td>C_L = 350 pF</td>
<td></td>
</tr>
<tr>
<td>t_{DB}</td>
<td>Delay to Base Drive to External PNP (Pin 12)</td>
<td>4</td>
<td>8</td>
<td>17</td>
<td>nS</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: 1. T_A = 25°C

A.C. CONDITIONS OF TEST:
Input Pulse Amplitudes: 3.0V  Input Pulse Rise and Fall Times: 5 nS between 1 volt and 2 volts  Measurement Points: See Waveforms
TTL Drivers

Since TTL devices will typically pull up actively to 2.8V to 3.4V, which is well above the required minimum high level, pull up resistors are not needed. Standard Series 7400 type gates are specified to supply 400 μA up level current at 2.4V worst case. Since each address input of the 2107B has a maximum leakage current of 10 μA, this type of driver is capable of driving 40 2107B address lines. However, it should be noted that these 40 address inputs have a capacitance of 240 pF. This load will increase the delay through the series 74 gates.

When driving the 2107B address inputs with TTL gates it is advisable to use a NAND type circuit.
(such as shown in Figure 31) with an enable input. This will allow all addresses to be set up in a high state (above 2.4V) and be driven low when appropriate. Since TTL gates have much better drive capability in the high to low direction, the increase in delay due to the large capacitance is reduced.

It is not recommended that Schottky type TTL gates be used to drive the low level inputs of the 2107B. This is because under worst case conditions, the down level of the Schottky device is approximately 100 mv higher than for a regular or H series TTL gate. This higher level coupled with the address noise coupled from the 2107B (see Address Buffer/Latch section) might make some systems marginal in operation. In addition, the effect of chip enable transition on address low voltage reduces the maximum positive down level on the addresses. (See Device Specification section.)

An example of TTL circuits (7400, 74H00, 74S00) driving 36 address inputs on the 2107B at refresh time is shown in Figure 32. Figure 33 shows the same TTL gate at “Read” time. Note the high level loading effect is greatly reduced because only 9 loads (2107B) are turned on at one time. Note that a Series 74S gate was used and is shown for reference only. From these photos the amount of overshoot present in driving high-low is clearly seen. Therefore, even with TTL drivers it is desirable to use series resistors to decrease the negative overshoot. This resistor value depends on the load on the driver and 20Ω is recommended when driving 36 address loads.

---

**Figure 32. TTL Driver Waveforms (Refresh Cycle)**

**Figure 33. TTL Driver Waveforms (Read Cycle)**
In the discussion of the address latch circuitry (Address Buffer/Latch section) reference was made to input currents drawn by the address buffer when an address is switched from a low to high level during chip enable. The decrease in high level shown in Figure 32 is due to the 0.5 mA/2107B loading of the address line following the low to high transition while chip enable is on. (All photos from Figure 32 are taken at refresh time when all devices are on. This condition is worst case.)

Figure 32 also shows the effect of 36 memory devices coupling charge back to the address line [see Note (1) on photos]. This coupling limits the series resistance value which can be added to the address drivers to minimize overshoot. It also suggests that the address drivers be placed as close as practical to the memory array.

The photo shown in Figure 34 is the current associated with the low to high level address transition for 36 devices at refresh time. (Note the time delay of current relative to address voltage change. This is the result of delays associated with the current probe relative to the voltage probe.) For this example, the driver used is a 3210.

Other Low Voltage Driver/Buffers

When speed and high level drive capability is needed it is desirable to use drivers which are designed specifically for driving high capacitance loads with minimum delay. The 3235 and 3210 can be used to drive the 2107B low voltage inputs.

When operating the 3235 in a low voltage mode, the device is connected per schematic shown in Figure 35. As shown in this figure, the VDD1 pin (pin 1) is connected to VCC (+5) and the VDD2 pin (pin 9) is connected to +12V. Photos of the waveforms of the 3235 in the low voltage drive mode are shown in Figure 36a and b. The circuit configuration is shown in Figure 35. As shown in the photo, the 3235 has very high drive capability in both the positive and negative directions.

For comparison, the low level buffer portions of the 3210 are shown in Figure 37a and b. As is shown, both the 3235 and 3210 make excellent low level buffer drivers for heavily loaded address lines.
Output Sensing

The output of the 2107B can be sensed with any TTL compatible series 74, 74L, 74LS or 74S gate. In addition, Intel provides a latch (3404) which features high speed and high density in a single package. The pin configuration for the 3404 is shown in Figure 38.

The \( V_{CC} \) input to the 2107B goes only to the output buffer as shown in Figure 8. This means that other types of outputs can be used instead of standard TTL devices if so desired. However, since there are many different ways to utilize this feature, do not exceed the maximum limits on voltage when using the 2107B in a non-standard manner.

Typical curves of output current as a function of output voltage are included in Figure 39a and b to facilitate the output interface of non-TTL loads.

System Timing and Control

The simplicity of design when using the 2107B memory component is shown by the schematic given in Figures 40, 41, and 42. The basic timing for this schematic is shown in Figure 43.

The design shown is for an expandable 16K X 18 system featuring:

1. Asynchronous memory requests/multiple ports
2. Free running refresh

The timing cycle consists of a start initiated by a memory request (MREQ) which triggers the busy latch and begins chip enable. The busy signal is used to disable other ports from requesting a memory cycle while the memory is being accessed from...
Figure 40. 16K X 18 Memory System Timing Generation
Figure 41. 16K X 18 Memory System Address Buffer Interface
However, several things need to be said about the refresh circuitry. As many system designers know, when a memory system with asynchronous refresh runs into trouble in the checkout state, it is 99% sure to be refresh interference in one form or another in the control logic. The most likely cause of problems for asynchronous refresh is glitching between a refresh request and a normal cycle request resulting in false starts or the system not knowing whether or not it is in a refresh cycle or normal cycle.

To alleviate this problem it is necessary to determine that there are no possible requests coming from an external port to the memory when a refresh cycle is started. This will prevent the low order address line from making transitions at the wrong time (due to the multiplexer between the refresh and normal addresses) and taking excessive time to recover to the proper level.

The circuit which performs the function of delaying the onset of a refresh cycle is shown by G3 in Figure 40. Here, refresh is delayed for as long as necessary to assure that the refresh required latch (REF REQ) has had time to block further requests from all ports attached to the memory.

Attention is also called to the power on reset (PWRST) signal shown in Figure 40. This signal is necessary to assure that all latches have been reset (or set) to the proper state after power has been applied. In addition, note that the refresh/addresses RA0 thru RA5 are changed after the
refresh cycle is complete. This assures that the address will not be changing during refresh as chip enable goes high.

**Memory Array Layout**

The layout for the 2107B memory array can be identical to that used for the 2107A. An example of such a layout is shown in Figure 44. The layout in this example is constructed with grided power busing which minimizes power distribution noise. When using this technique it is important to remember to bus all power lines both vertically and horizontally through every memory component.

The effect of proper power distribution in the memory array cannot be over-emphasized. It is most desirable to bus the power lines both vertically and horizontally at every memory device location (even if it means running a 15 mil wide printed line to achieve the connection). If it is not possible to make such a connection at every location, then the interconnect should be done as much as possible throughout the array.

As a general rule of thumb, power distribution can be considered adequate if the distance from each power pin (e.g., V_DD to capacitor and V_SS to capacitor) to the closest decoupling capacitor is less than or equal to 1.5 inches.

For some layouts, particularly those which have all timing and control as well as the memory on a single board, it may be desirable to build multilayer boards. Attention should be paid to the construction of the internal planes to gain maximum effectiveness from these planes. If all the required power supplies cannot be distributed on internal
planes and any have to be left out and put on the upper surfaces of the board they should be removed from the internal plane in the following order:

1. \( V_{CC} \) 3. \( V_{DD} \)
2. \( V_{BB} \) 4. \( V_{SS} \)

Numbers 1 and 2 can be interchanged if there is a particularly heavy \( V_{CC} \) load due to timing, control, etc. circuitry on the board.

When constructing internal planes, care should be taken to obtain the most continuous plane possible. For example, the plane should have "fingers" between each IC feedthrough to minimize inductance.

**Decoupling**

As mentioned in the Transient Currents section, it is imperative to adequately decouple all supplies to the 2107B. The type and amount of decoupling recommended is most easily shown with the aid of the diagram given in Figure 45. In this figure, every other location for decoupling is \( V_{DD} \) - \( V_{SS} \) using a 1.0 \( \mu F \) capacitor. Alternate locations can be \( V_{BB} \) - \( V_{SS} \) or \( V_{CC} \) - \( V_{SS} \). It is suggested that \( V_{BB} \) - \( V_{SS} \) be decoupled more heavily than \( V_{CC} \) - \( V_{SS} \) (as shown in Figure 45), because of the higher transients on \( V_{BB} \). Noise on the \( V_{BB} \) distribution is shown in Figure 46.

In addition to the 1.0 \( \mu F \) decoupling discussed above, it is necessary to provide a bulk of \(~100 \ \mu F\) \( V_{DD} \) - \( V_{SS} \) per 36 devices located near the memory array. Also, placing 4.7 \( \mu F \) capacitors between \( V_{DD} \) - \( V_{SS} \) along the end of each row as shown will eliminate noise problems during refresh time.

The effect of changing decoupling capacitance in a system is shown in Figure 47a, b, c, and d.

These photos show the effects of different decoupling schemes on the \( V_{DD} \) supply and the effect of adding a more solid power distribution bus. (In this case #22 wire was paralleled with the existing power distribution of grided 15 mil printed line.) Each of the photos shown in Figure 47 were taken at the worst case location in the memory array at refresh time.

Figure 47a shows the \( V_{DD} \) supply with 0.1 \( \mu F \) spaced at every third device, no additional \( V_{DD} \) busing and no bulk capacitors (4.7 \( \mu F \)) at the end of each row. Note that the \( V_{DD} \) supply decreases to approximately 300 mv below desired setting with spikes driving the supply down a maximum of 440 mv. This excursion is not acceptable.

Figure 47b is for the condition of decoupling with 0.1 \( \mu F \) every third device and adding a 4.7 \( \mu F \) capacitor at the end of each row. Additional power busing on the \( V_{DD} \) and \( V_{SS} \) lines was added but was observed to have little effect on the noise, shown in Figure 47b. For this case, the \( V_{DD} \) supply is observed to decrease approximately 180 mv with spikes adding a further reduction to 240 mv. The major difference between this condition and the one shown in Figure 47a is the addition of the 4.7 \( \mu F \) capacitors at the end of each row. However, the decrease in \( V_{DD} \) voltage is still unacceptable.
Figure 47c shows the V_{DD} supply where V_{DD} in the memory array is decoupled at every other memory device location. All other conditions are per Figure 47b. Note that the offset is now only 100 mV with spikes taking the supply down to 170 mV below nominal. Such decoupling results in adequate but marginally acceptable system operation.

Figure 47d shows the V_{DD} supply decoupled at every other memory device location with 1.0 μF ceramic capacitors. All other conditions are per Figure 47c. Note that the offset is approximately 20 mV with spikes lowering the V_{DD} to a maximum of 200 mV for the length of time shown.

The most desirable decoupling of V_{DD} to V_{SS} in a memory array is therefore 1.0 μF at every other device location with 4.7 μF at the end of each row.

The above recommendations on power distribution and decoupling will result in minimal memory array power noise. However, it is certainly not the only way to suppress power distribution noise. Adequate distribution and decoupling can be assumed if the following values are achieved:

1. V_{DD}−V_{SS} 200 mV peak
2. V_{BB}−V_{SS} 100 mV peak
3. V_{CC}−V_{SS} 100 mV peak
4. V_{SS}−V_{SS} 200 mV peak (corner to diagonal corner)

Debugging A Memory System

The design and build of memory systems using the newer, easier to use dynamic RAMs, usually results in minimum system debugging time. However, when this is not the case and the control and memory are not playing together well, life can be mighty miserable for the designer while the problem is being tracked down.

This section will deal with some of the more common problems that can affect dynamic memory systems in general, their characteristics and how to better identify them. An integral part of this section is the testing of the system to identify those conditions which cause the most problems for the memory system. In the following it is assumed that power supplies and timing are set to nominal values.

In debugging a memory system the most logical place to start is to determine that all specified criteria are met. This means looking at chip enable timing during each type of cycle both high and low
voltage level (read, write, read-modify-write, if used, and refresh). In all cycles make sure the addresses and chip select are set up at the proper time and are held for the minimum hold time. Check all other signals for proper levels (this especially includes the address down level at the time just after chip enable goes high). Remember that the maximum address down level is a function of the chip enable rise time. Erratic operation results from a slow transition and a marginal address down level. Next, check all voltage pins for excessive noise. It is usually desirable to check the power noise at refresh time since all memory devices will be on then and noise will be at a maximum.

After the above, sync on a read cycle and make sure that the system data strobe, if any, occurs before chip enable going low has a chance to reset the data. Also check to make sure no spurious write signals are getting through at read time. In a write cycle check the write enable waveform and make sure data-in is valid at or before write enable goes low.

In a refresh cycle, write enable should be held high unless chip select is high. Also, while in the refresh mode, make sure that all refresh addresses are being accessed. This is most easily done by syncing on the high order refresh address, A5, and looking at the low order addresses for one cycle of A5. Checking a read-modify-write cycle is merely a combination of the above discussion of read and write.

After confirming that the specification is met in all regards and that power supply noise is within tolerance in all cycles, the designer is probably tempted to harbor ill feelings toward the memory component and/or manufacturer of same. However, it is not yet time for such.

If the memory is failing most of the data and address patterns that are being used for the test, it is useful to inhibit refresh. When doing so, make sure that the test cycle is such that refresh is being done “automatically” by the normal cycles occurring at a fast enough rate. When inhibiting refresh it may be necessary to restrict the test addressing so that all cells can be “refreshed” by a normal cycle. If the problem goes away after inhibiting refresh, you are now in the army of people who have used dynamic RAMs to be caught with refresh interference.

The only thing that can be said about refresh interference is that refresh is coming in at the wrong time! In properly designed systems, the most likely culprit is a noise glitch getting into the refresh timing circuitry to cause the problem. One of the most common causes for other types of system design is the improper use of “D” type latches. For example, if an asynchronous input (relative to clock) is applied to the D input of a latch and clocked, there will be times where the change on the D input occurs simultaneously with the clock. In some latches this can cause an order of magnitude increase in delay instead of simply missing the D input (see Figure 48). This problem also exists when using a latch made of NAND gates (see Figure 49). The method of correcting the refresh interference problem of a system is left to the imagination and luck of the designer. If the problem is not refresh interference, do not harbor ill feelings yet!

After checking all of the above with no change in results, the next place to start is to determine whether the system is sensitive to addressing patterns. An effective test for evaluating address pattern sensitivity is Galpat. The structure of Galpat is shown in Figure 50. This test is time consuming and requires a careful monitoring of the failed data and its addresses.

Failures caused by a Galpat-only type test are most likely due to address line noise, address coupling to other signals, or refresh related. If address type noise is suspected a careful look at every point in each address path is in order. The best place to concentrate is around the address and its complement that failed.

Refresh related problems can occur during Galpat because this test takes a long time and may not “automatically” refresh the memory. (A sequential type test can refresh the memory automatically if it cycles faster than the maximum allowed
A “galloping” “1” or “0” thru memory consists of initializing the contents of memory (all “1s” or “0s”) and implementing the following sequence at each successive memory location:

1. Write opposite data (from initialized state) into test address (A\text{TEST})
2. Read next address (A\text{TEST} + 1)
3. Read test address (A\text{TEST})
4. Read A\text{TEST} + 2
5. Read test address — continue read sequence for entire memory
6. Write test address back to initialize state
7. Go to next address for new A\text{TEST}
8. Repeat steps 1–6 until entire memory tested
9. Complement initial data pattern and repeat steps 1–8

**Figure 50. Galpat Flow Chart**

---

refresh period.) If any address fails to get refreshed during the refresh period, Galpat will most likely pick it up.

If the above does not yield a clue, then a check of the data pattern across a word is in order. In many tests each bit in a word contains the same data. This can cause certain groups of data lines to couple into adjacent control or address lines. This problem can be tracked down by allowing only one bit in a word to change at a time.

If the memory system is having massive failures, it is very likely that the above debug procedure will reveal the problem. The second type of problem to be discussed is that of soft failures at frequent intervals. In general, these are problems caused by system noise, marginal timing, flaky peripheral device(s), or marginal memory component.

For soft failures, the first item to suspect is refresh interference. Proceed per above to isolate the problem.

A great deal of information on soft failures at nominal voltage settings can be obtained by shmooring the memory system. A shmoo consists of varying each voltage in a manner which is worst case for certain conditions.

The voltage points which emphasize certain tendencies in the memory are contained in Figure 51. The device failed address should be noted at each shmoo point to give a clue to the problem.

---

**A broad guideline here is as follows:**

<table>
<thead>
<tr>
<th>Failure</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. V\text{DD} low,</td>
<td></td>
</tr>
<tr>
<td>V\text{BB}} high</td>
<td></td>
</tr>
<tr>
<td>2. V\text{DD} high,</td>
<td></td>
</tr>
<tr>
<td>V\text{BB}} low</td>
<td>Look for V\text{SS}, V\text{DD}, V\text{BB noise.}</td>
</tr>
</tbody>
</table>

Temperature variation can also reveal similar problems. For example:

<table>
<thead>
<tr>
<th>Failure</th>
<th>Cause</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. High temperature</td>
<td></td>
</tr>
<tr>
<td>2. Low temperature</td>
<td></td>
</tr>
</tbody>
</table>

---

**Figure 51. Example of Memory System Shmoo Plot**

---

**Power Calculations**

The typical power dissipation for the 2107B with a chip enable on time of 230 nsec and a 400 nsec cycle is calculated as follows for a typical device:

**Device Power**

\[ \text{PDOP} = \left[ \frac{\text{VDD} \times \text{IDD1AV}}{\text{VBB} \times \text{IBB}} \right] \]

\[ = \left[ \frac{12.0 \times 55 \text{ mA}}{5.0 \times 0.1 \text{ mA}} \right] = 660 \text{ mw} \]

Since the calculation of standby power without refresh for dynamic memory is meaningless, the following calculations are for standby with refresh:

\[ \text{PDOP} = \left[ \frac{\text{VDD} \times \text{IDD1}}{\text{VBB} \times \text{IBB}} \right] \]

\[ = \left[ \frac{12.0 \times 0.11 \text{ mA}}{5.0 \times 0.1 \text{ mA}} \right] = 1.82 \text{ mw} \]
3. \[ P_{DSB} = P_{DOP} \left( \frac{N \cdot T_{CY}}{T_{REF}} \right) + P_{NOP} \left( \frac{T_{REF} - N \cdot T_{CY}}{T_{REF}} \right) \]

where:
- \( P_{DOP} \) = Operating power dissipation
- \( P_{NOP} \) = Non-operating (chip enable low) power dissipation
- \( P_{DSB} \) = Standby/Refresh power
- \( N \) = Number of refresh cycles in refresh period
- \( T_{REF} \) = Refresh period in \( \mu \text{sec} \)
- \( T_{CY} \) = Refresh cycle time in \( \mu \text{sec} \)

For the 2107B, the following values apply:
- \( N = 64 \)
- \( T_{REF} = 2000 \mu \text{sec} \)
- \( T_{CY} = 0.40 \mu \text{sec} \)

4. \[ P_{DSB} = 660 \left( \frac{64(0.400)}{2000} \right) + 1.82 \left( \frac{2000-25.6}{2000} \right) \text{mw} \]

or

5. \( P_{DSB} = (8.45 + 1.80) \text{ mw} \)

6. \( P_{DSB} = 10.3 \text{ mw} \)

The above calculations do not include \( V_{CC} \) power since it is dependent only upon the output load used. The output of the 2107B is in a high impedance state when chip enable is low or chip select is high and only leakage level currents flow under these conditions.

**System Power**

In most systems only a portion of the memory devices will be continually accessed. For example, in the system previously described (16K X 18) worst case power is a continual access of one row (the other three rows are dissipating power in the refresh only mode).

System power for the 16K X 18 system is calculated from:

1. \[ P_{SYS} = P_{DS} \times N + P_{DA} \times M + P_{DOP} \times D + P_{DSB} \times E \]

where:
- \( P_{DS} \) = Power dissipated in drivers during standby (including refresh)
- \( N \) = Number of drivers in standby
- \( P_{DA} \) = Power dissipated in drivers during max. duty cycle operation
- \( M \) = Number of drivers in max. duty cycle operation
- \( P_{DOP} \) = Power dissipated by memory device max. duty cycle
- \( D \) = Number of devices in \( P_{DOP} \)
- \( P_{DSB} \) = Power dissipated by memory devices during standby (including refresh)
- \( E \) = Number of devices in \( P_{DSB} \)

For this example, all drivers are assumed to be 3210s. Therefore:
- \( P_{DS} = 387 \text{ mw} \)
- \( N = 6 \)
- \( P_{DA} = 467 \text{ mw} \)
- \( M = 2 \)
- \( P_{DOP} = 660 \text{ mw} \)
- \( D = 18 \)
- \( P_{DSY} = 10.3 \text{ mw} \)

or

\[ P_{SYS} = 387 (6) + 467 (2) + 660 (18) + 10.3 (54) \]

The power dissipated by the drivers is approximately 26% of total system power in a max.-duty cycle operating environment.

Total standby power (including refresh is calculated from equation (1) where:
- \( N = 8 \)
- \( M = 0 \)
- \( D = 0 \)
- \( E = 72 \)

or:

\[ P_{SYS} = 387 (8) + 10.3 (72) \]

\[ P_{SYS} = (3096 + 742) \text{ mw} \]

or

\[ P_{DRIVERS} = 3092 \text{ mw} \]
\[ P_{MEMORY} = 742 \text{ mw} \]

5. \( P_{SYS} = 3.83 \text{ watts} \)

Note that in this case, driver power amounts to approximately 81% of total system power.

**Power Supply Sequencing**

The \( V_{BB} \) substrate bias supply must never be allowed to be more positive than 0.3V above \( V_{SS} \), \( V_{DD} \), or \( V_{CC} \) at any time. Catastrophic device failure can result if these criteria are not met. To minimize this problem of power sequencing and inadvertent power shorts, it is recommended that \( V_{BB} \) be referenced to \( V_{SS} \).

**ACKNOWLEDGMENT**

Appreciation is extended to R. L. Papenburg of the Application Engineering Department for his work on the 3235 and 3210 driver system evaluation.
FULLY DECODED RANDOM ACCESS
4096 BIT DYNAMIC MEMORY

- Access Time -- 200 ns max.
- Read, Write Cycle Times -- 400 ns max.
- Refresh Period -- 2 ms

- Low Cost Per Bit
- Low Standby Power
- Easy System Interface
- Only One High Voltage Input Signal -- Chip Enable
- TTL Compatible -- All Address, Data, Write Enable, Chip Select Inputs
- Read-Modify-Write Cycle Time -- 520 ns
- Address Registers Incorporated on the Chip
- Simple Memory Expansion -- Chip Select Input Lead
- Fully Decoded -- On Chip Address Decode
- Output is Three State and TTL Compatible
- Industry Standard 22-Pin Configuration

The Intel 2107B is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107B uses dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is non-destructive. Refreshing is most easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107B is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies. The 2107B uses a single transistor cell to achieve high speed and low cost. It is a replacement for the 2107A.
## Absolute Maximum Ratings*

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limits</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Under Bias</td>
<td>0°C to 70°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
<td></td>
</tr>
<tr>
<td>All Input or Output Voltages with Respect to the most Negative Supply Voltage, ( V_{BB} )</td>
<td>+25V to -0.3V</td>
<td></td>
</tr>
<tr>
<td>Supply Voltages ( V_{DD}, V_{CC}, ) and ( V_{SS} ) with Respect to ( V_{BB} )</td>
<td>+20V to -0.3V</td>
<td></td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>1.25W</td>
<td></td>
</tr>
</tbody>
</table>

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. and Operating Characteristics

\( T_A = 0°C \) to 70°C, \( V_{DD} = +12V \pm 5\% \), \( V_{CC} = +5V \pm 5\% \), \( V_{BB}[^1] = -5V \pm 5\% \), \( V_{SS} = 0V \), unless otherwise noted.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Limits</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{LI} )</td>
<td>Input Load Current (all inputs except CE)</td>
<td>Min.</td>
<td>Typ.[2]</td>
<td>Max.</td>
</tr>
<tr>
<td>( I_{LC} )</td>
<td>Input Load Current</td>
<td>.01</td>
<td>10</td>
<td>( V_I = V_{IL} ) MIN to ( V_{IH} ) MAX</td>
</tr>
<tr>
<td>( I_{LO} )</td>
<td>Output Leakage Current for high impedance state</td>
<td>.01</td>
<td>10</td>
<td>( V_I = V_{ILC} ) or ( V_I = V_{IH} ) ( V_O = 0V ) to 5.25V</td>
</tr>
<tr>
<td>( I_{DD1} )</td>
<td>( V_{DD} ) Supply Current during CE off[^3]</td>
<td>110</td>
<td>200</td>
<td>( V_I = -1V ) to +.6V</td>
</tr>
<tr>
<td>( I_{DD2} )</td>
<td>( V_{DD} ) Supply Current during CE on</td>
<td>80</td>
<td>100</td>
<td>( V_O = 0V )</td>
</tr>
<tr>
<td>( I_{DD AV1} )</td>
<td>Average ( V_{DD} ) Current</td>
<td>55</td>
<td>80</td>
<td>( V_O = 0V )</td>
</tr>
<tr>
<td>( I_{DD AV2} )</td>
<td>Average ( V_{DD} ) Current</td>
<td>27</td>
<td>40</td>
<td>( V_O = 0V )</td>
</tr>
<tr>
<td>( I_{CC1}[^4] )</td>
<td>( V_{CC} ) Supply Current during CE off</td>
<td>.01</td>
<td>10</td>
<td>( V_I = V_{ILC} ) or ( V_I = V_{IH} )</td>
</tr>
<tr>
<td>( I_{BB} )</td>
<td>( V_{BB} ) Supply Current</td>
<td>5</td>
<td>100</td>
<td>( V_I = V_{ILC} ) or ( V_I = V_{IH} )</td>
</tr>
<tr>
<td>( V_I )</td>
<td>Input Low Voltage</td>
<td>-1.0</td>
<td>0.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ILC} )</td>
<td>CE Input Low Voltage</td>
<td>2.4</td>
<td>V_{CC}+1</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>Input High Voltage</td>
<td>-1.0</td>
<td>+1.0</td>
<td>V</td>
</tr>
<tr>
<td>( V_{ILC} )</td>
<td>CE Input High Voltage</td>
<td>0.0</td>
<td>0.45</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Low Voltage</td>
<td>2.4</td>
<td>V_{CC}</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output High Voltage</td>
<td>2.4</td>
<td>V_{CC}</td>
<td>V</td>
</tr>
</tbody>
</table>

**NOTES:**

1. The only requirement for the sequence of applying voltage to the device is that \( V_{DD}, V_{CC}, \) and \( V_{SS} \) should never be 3V more negative than \( V_{BB} \).
2. Typical values are for \( T_A = 25°C \) and nominal power supply voltages.
3. The \( I_{DD} \) and \( I_{CC} \) currents flow to \( V_{SS} \). The \( I_{BB} \) current is the sum of all leakage currents.
4. During CE on \( V_{CC} \) supply current is dependent on output loading, \( V_{CC} \) is connected to output buffer only.
Typical Characteristics

Fig. 1. Typical $I_{DDAV1}$ vs. Temperature

Fig. 2. Typical $I_{DDAVG}$ vs. Cycle Time

Fig. 3. Typical $I_{DD2}$ vs. Temperature

Fig. 4. Typical $V_L$ MAX vs. CE Rise Time

Fig. 5. Typical $I_{OH}$ vs. $V_{OH}$

Fig. 6. Typical $I_{OL}$ vs. $V_{OL}$

Fig. 7. Typical Refresh vs. Temperature

Fig. 8. Typical Access Time vs. Temperature
A.C. Characteristics \(^{[1]}\) \(T_A = 0^\circ\text{C to } 70^\circ\text{C}, \quad V_{DD} = 12V \pm 5\%, \quad V_{CC} = 5V \pm 5\%, \quad V_{BB} = -5V \pm 5\%, \)

READ, WRITE, AND READ MODIFY/WRITE CYCLE \(V_{SS} = 0V, \text{ unless otherwise noted.}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{REF})</td>
<td>Time Between Refresh</td>
<td>2</td>
<td>ns</td>
<td></td>
<td>(t_{AC}) is measured from end of address transition</td>
</tr>
<tr>
<td>(t_{AC})</td>
<td>Address to CE Set Up Time</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{AH})</td>
<td>Address Hold Time</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{CC})</td>
<td>CE Off Time</td>
<td>130</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{T})</td>
<td>CE Transition Time</td>
<td>10</td>
<td>40</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>(t_{CF})</td>
<td>CE Off to Output High Impedance State</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**READ CYCLE**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{CY})</td>
<td>Cycle Time</td>
<td>400</td>
<td>ns</td>
<td></td>
<td>(t_{T} = 20\text{ns})</td>
</tr>
<tr>
<td>(t_{CE})</td>
<td>CE On Time</td>
<td>230</td>
<td>3000</td>
<td>ns</td>
<td>(C_{load} = 50\text{pF}, \text{ Load = One TTL Gate,}) ( \text{Ref = 2.0V})</td>
</tr>
<tr>
<td>(t_{CO})</td>
<td>CE Output Delay</td>
<td>180</td>
<td>ns</td>
<td></td>
<td>(t_{ACC} = t_{AC} + t_{CO} + 11t_{T})</td>
</tr>
<tr>
<td>(t_{ACC})</td>
<td>Address to Output Access</td>
<td>200</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{WL})</td>
<td>CE to WE</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{WC})</td>
<td>WE to CE on</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**WRITE CYCLE**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{CY})</td>
<td>Cycle Time</td>
<td>400</td>
<td>ns</td>
<td></td>
<td>(t_{T} = 20\text{ns})</td>
</tr>
<tr>
<td>(t_{CE})</td>
<td>CE On Time</td>
<td>230</td>
<td>3000</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>(t_{W})</td>
<td>WE to CE Off</td>
<td>150</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{CW})</td>
<td>CE to WE</td>
<td>100</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{DW}^{[2]})</td>
<td>D(_{IN}) to WE Set Up</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{DH})</td>
<td>D(_{IN}) Hold Time</td>
<td>0</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{WP})</td>
<td>WE Pulse Width</td>
<td>50</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Capacitance \(^{[3]}\) \(T_A = 25^\circ\text{C}\)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test</th>
<th>Plastic And Ceramic Pkg. Pkg.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>(C_{AD})</td>
<td>Address Capacitance, (CS)</td>
<td>4</td>
<td>6</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{CE})</td>
<td>CE Capacitance</td>
<td>17</td>
<td>25</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{OUT})</td>
<td>Data Output Capacitance</td>
<td>5</td>
<td>7</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{IN})</td>
<td>(D_{IN}) and WE Capacitance</td>
<td>8</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

Notes:
1. A.C. characteristics are guaranteed only if cumulative CE on time during \(t_{REF}\) is <60% of \(t_{REF}\).
2. If WE is low before CE goes high then \(D_{IN}\) must be valid when CE goes high.
3. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation
\[
C = \frac{1}{\Delta t}\frac{\Delta V}{\Delta V}
\] with the current equal to a constant 20mA.
Read and Refresh Cycle \(^1\) (Numbers in parentheses are for minimum cycle timing in ns)

Write Cycle

NOTES:
1. For Refresh cycle row and column addresses must be stable before \(t_{AC}\) and remain stable for entire \(t_{AH}\) period.
2. \(V_{IL\ MAX}\) is the reference level for measuring timing of the addresses, \(CS\), \(WE\), and \(DIN\).
3. \(V_{IH\ MIN}\) is the reference level for measuring timing of the addresses, \(CS\), \(WE\), and \(DIN\).
4. \(V_{SS} +2.0V\) is the reference level for measuring timing of \(CE\).
5. \(V_{DD} -2V\) is the reference level for measuring timing of \(CE\).
6. \(V_{GS} +2.0V\) is the reference level for measuring the timing of \(DOUT\).
7. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.
**Read Modify Write Cycle**[1]

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>t(_{RWC})</td>
<td>Read Modify Write(RMW) Cycle Time</td>
<td>520 ns</td>
<td></td>
<td></td>
<td>t(_T) = 20ns</td>
</tr>
<tr>
<td>t(_{CRW})</td>
<td>CE Width During RMW</td>
<td>350 ns</td>
<td>3000 ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>t(_{WC})</td>
<td>WE to CE on</td>
<td>0 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{W})</td>
<td>WE to CE off</td>
<td>150 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{WP})</td>
<td>WE Pulse Width</td>
<td>50 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{DW})</td>
<td>D(_{IN}) to WE Set Up</td>
<td>0 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{DH})</td>
<td>D(_{IN}) Hold Time</td>
<td>0 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{CO})</td>
<td>CE to Output Delay</td>
<td>180 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>t(_{ACC})</td>
<td>Access Time</td>
<td>200 ns</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Numbers in parentheses are for minimum cycle timing in ns.)

**NOTES:**
1. A.C. characteristics are guaranteed only if cumulative CE on time during t\(_{REF}\) is ≤60% of t\(_{REF}\). For continuous Read-Modify-Write operation t\(_{CC}\) and t\(_{RWC}\) should be increased to at least 195ns and 585 ns, respectively.
2. V\(_{IL\_MAX}\) is the reference level for measuring timing of the addresses, CS, WE, and D\(_{IN}\).
3. V\(_{IH\_MIN}\) is the reference level for measuring timing of the addresses, CS, WE, and D\(_{IN}\).
4. V\(_{SS}\) +2.0V is the reference level for measuring timing of CE.
5. V\(_{DD}\) -2V is the reference level for measuring timing of CE.
6. V\(_{DD}\) -2V is the reference level for measuring the timing of D\(_{OUT}\).
7. WE must be at V\(_{IH}\) until end of t\(_{CO}\).
8. During CE high typically 0.5mA will be drawn from any address pin which is switched from low to high.
Applications

Refresh

The 2107B is refreshed by either a read cycle, write cycle, or read-modify write cycle. Only the selected row of memory array is refreshed. The row address is selected by the input signals A0 thru A5. Each individual row address must receive at least one refresh cycle within any two milliseconds time period.

If a read cycle is used for refreshing, then the chip select input, \( \overline{CS} \), can be a logic high or a logic low. If a write cycle or read-modify write cycle is used to refresh the device, then \( \overline{CS} \) must be a logic high. This will prevent writing into the memory during refresh.

Power Dissipation

The operating power dissipation of a selected device is the sum of \( V_{DD} \times I_{DDA} \) and \( V_{BB} \times I_{BB} \). For a cycle of 400ns and \( t_{CE} \) of 230ns typical power dissipation is 660mW.

Standby Power

The 2107B is a dynamic RAM therefore when \( V_{CE} = V_{ILC} \) very little power is dissipated. In a typical system most devices are in standby with \( V_{CE} \) at \( V_{ILC} \). During this time only leakage currents flow (i.e., \( I_{DD1}, I_{CC1}, I_{BB}, I_{LO}, I_{L1} \)). The power dissipated during this inactive period is typically 1.4mW. The typical power dissipation required to perform refresh during standby is the refresh duty cycle, 1.3%, multiplied by the operating power dissipation, or 8.6mW. The total power dissipation during standby is then 10.0mW typical.

System Interfaces and Filtering

On the following page is an example of a 16K x 9 bit memory system. Device decoding is done with the CE input. All devices are unselected during refresh with \( \overline{CS} \). The 3210, 3230, 3235, and 3404 are standard Intel products. Decoupling is indicated by "1" for \( V_{DD} \) to \( V_{SS} \) and "2" for \( V_{BB} \) to \( V_{SS} \). \( I_{DD} \) and \( I_{BB} \) current surges at the CE transitions make adequate decoupling of these supplies important. It is recommended that 1\( \mu \)F high frequency, low inductance capacitors be used on double sided boards. \( V_{CC} \) to \( V_{SS} \) decoupling is required only on the devices located around the periphery of the array. For each 36 devices a 100\( \mu \)F tantalum or equivalent capacitor should be placed from \( V_{DD} \) to \( V_{SS} \) close to the array.
Typical System

16K x 9 BIT MEMORY CIRCUIT

Packaging Information

22-LEAD CERAMIC DUAL IN-LINE PACKAGE OUTLINE (C)
## 2107B SELECTION GUIDE

<table>
<thead>
<tr>
<th>INTEL PART NO.</th>
<th>MAXIMUM ACCESS TIME (ns)</th>
<th>MINIMUM READ OR WRITE CYCLE (ns)</th>
<th>MINIMUM RMW CYCLE (ns)</th>
<th>REFRESH TIME (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2107B</td>
<td>200</td>
<td>400</td>
<td>520</td>
<td>2</td>
</tr>
<tr>
<td>2107B-4</td>
<td>270</td>
<td>470</td>
<td>590</td>
<td>2</td>
</tr>
<tr>
<td>2107B-6</td>
<td>350</td>
<td>800</td>
<td>960</td>
<td>1</td>
</tr>
</tbody>
</table>

Intel sells a complete line of memory and microprocessor components. In addition, Intel Memory Systems, located in Sunnyvale, California, designs and manufacturers memory cards, add-on memories, and complete memory systems. For more information about these components or memory systems, contact your local Intel sales representative.