87C196CB Specification Update

Automotive

October 1998

Notice: The 87C196CB may contain design defects or errors known as errata. Characterized errata that may cause the 87C196CB's behavior to deviate from published specifications are documented in this specification update.

Order Number: 273152-002

Contents

Revision History

Date	Version	Description
1/12/98	001	This is the new Specification Update document. It contains all errata published prior to this date.
10/28/98	002	Added Specification Change 2.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order #
87C196CB Supplement to 8XC196NT User's Manual	272787
87C196CB 20MHz Advanced 16-Bit CHMOS Microcontroller with Integrated CAN 2.0 datasheet.	272405

Nomenclature

Errata are design defects or errors. These may cause the Product Name's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

▌	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings			Page	Status	ERRATA
	#	#	#			
						None for this revision of this specification update.

Specification Changes

No.	Steppings			Page	Status	SPECIFICATION CHANGES
	A	B	#			
1		X		7		Digital and Analog Supply Voltage Operating Conditions
2	X	X		7		Correction to Voh1 - Should be a Minimum Specification

Specification Clarifications

No.	Steppings			Page	Status	SPECIFICATION CLARIFICATIONS
	A	B	#			
1	X	X		8		CAN Interrupt Pending Register Check at End of ISR
2	X	X		8		CAN Interrupt Considerations when using Nohau CA/CB Emulator

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	272787-001	9	Doc	Table 10-3. Auto Programming Memory Map, Page 10-2
2	272787-001	10	Doc	Figure 10-1. Auto Programming Circuit, Page 10-3
3	272787-001	11	Doc	Appendix A; Signal Descriptions

Identification Information

Markings

AN87C196CB, AS87C196CB.

Errata

None in this specification update revision.

Specification Changes

1. Digital and Analog Supply Voltage Operating Conditions

Issue: The V_{CC} (Digital Supply Voltage) and Vref (Analog Supply Voltage) Operating Conditions have been revised from 4.5 V-5.5 V to 4.75 V-5.25 V.

Implication: The operating conditions for the digital and analog power supplies on the device are now specified to only tolerate a 5% deviation from the 5 V power supply in the application as opposed to the previous 10% deviation tolerance.

Affected Docs: 8*7C196CB 20 MHz Advanced 16-Bit CHMOS Microcontroller with Integrated CAN 2.0* datasheet - 272405.

2. Correction to Voh1 - Should be a Minimum Specification

Issue: The specification for Voh1, in datasheet 272405, is incorrectly indicated as a Maximum Specification of 2 V. This should be a Minimum Specification of 2 V.

Affected Docs: 8*7C196CB 20 MHz Advanced 16-Bit CHMOS Microcontroller with Integrated CAN 2.0* datasheet - 272405.

Specification Clarifications

1. CAN Interrupt Pending Register Check at End of ISR

Issue: When servicing CAN interrupts, the application must ensure that the interrupt register in the CAN contains no pending events before exiting the interrupt service routine (ISR). This is accomplished by checking the CAN Interrupt Register (1E5Fh) to make sure this register contains 00h prior to exiting the CAN ISR.

Implication: Failure to service all pending CAN interrupts before exiting the CAN ISR will result in an interrupt lockout condition. This lockout affects CAN interrupts only, and will block future CAN events from occurring in the CPU.

Workaround: (Software) Before exiting the CAN ISR, the CAN Interrupt Register should be read and the ISR should only be exited if this register is set to 00h. If not, service all remaining pending interrupts and then re-check the register to make sure it is set to 00h.

Affected Docs: *87C196CB Supplement to 8XC196NT User's Manual* - 272787.

2. CAN Interrupt Considerations when using Nohau CA/CB Emulator

Issue: The emulator device for the CB exhibits a CAN interrupt behavior which is different from the actual CB production device. This is a result of the internal interrupt signal from the CAN module being a level active signal on the emulator device, as opposed to a pulse active signal on the CB production device.

Implication: The difference between the CB emulator device and the CB production device will result in an additional "dummy" interrupt on the emulator device which occurs when the CAN interrupt service routine is exited.

Workaround: (Software) To prevent the "dummy" interrupt from occurring on the emulator device, the following procedure should be followed in the CAN interrupt service routine:

1. Identify the interrupt source (message object #, or status).
2. Service all interrupts within the CAN until the interrupt register contains 00h.
3. Clear the CANINT bit in the CPU Interface register.
4. Return from interrupt.

Clearing the CANINT bit in the CPU interrupt register will prevent the "dummy" interrupt from occurring when using the emulator. For the production CB, it is not necessary to clear the CANINT bit.

Affected Docs: *87C196CB Supplement to 8XC196NT User's Manual* - 272787.

Documentation Changes

1. Table 10-3. Auto Programming Memory Map, Page 10-2

Issue: Corrected programming pulse width (PPW) location.

Changed:

- "4014H" to "405EH"
- "4015H" to "405FH"
- "00014H" to "0005EH"
- "00015H" to "0005FH"

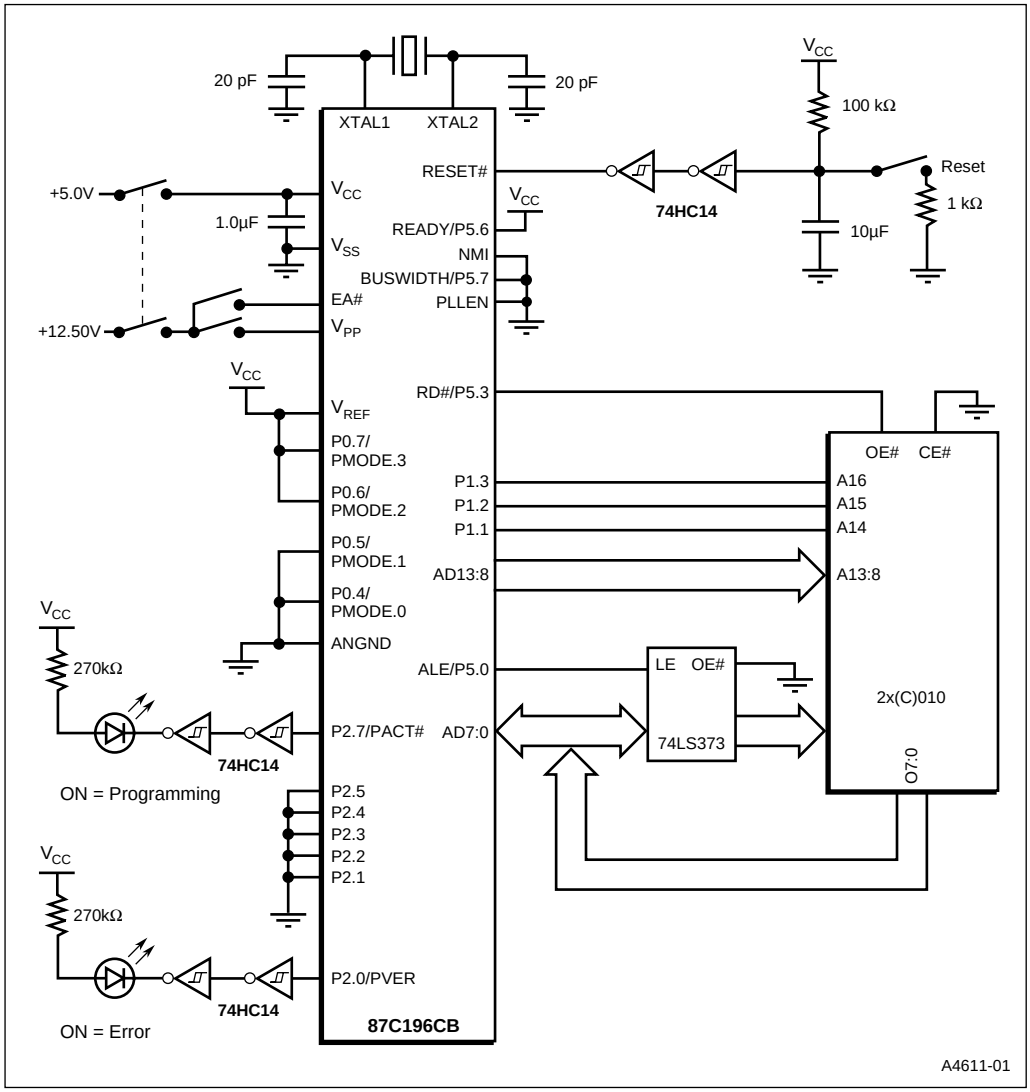
Address Output from 87C196CB (A15:0)	Internal OTPROM Address	Address Using Circuiting in Figure 10-1 (P1.3:1, A13:0)	Description
405EH	N/A	0005EH	Programming pulse width (PPW) LSB.
405FH	N/A	0005FH	Programming pulse width (PPW) MSB.

Affected Docs: *87C196CB Supplement to the 8XC196NT User's Manual* - 272787.

2. Figure 10-1. Auto Programming Circuit, Page 10-3

Issue: Corrections made in diagram (see below):

- PLLEN (pin 74) tied to V_{SS}
- Change external EPROM (27C512) to 27C010 (128K)

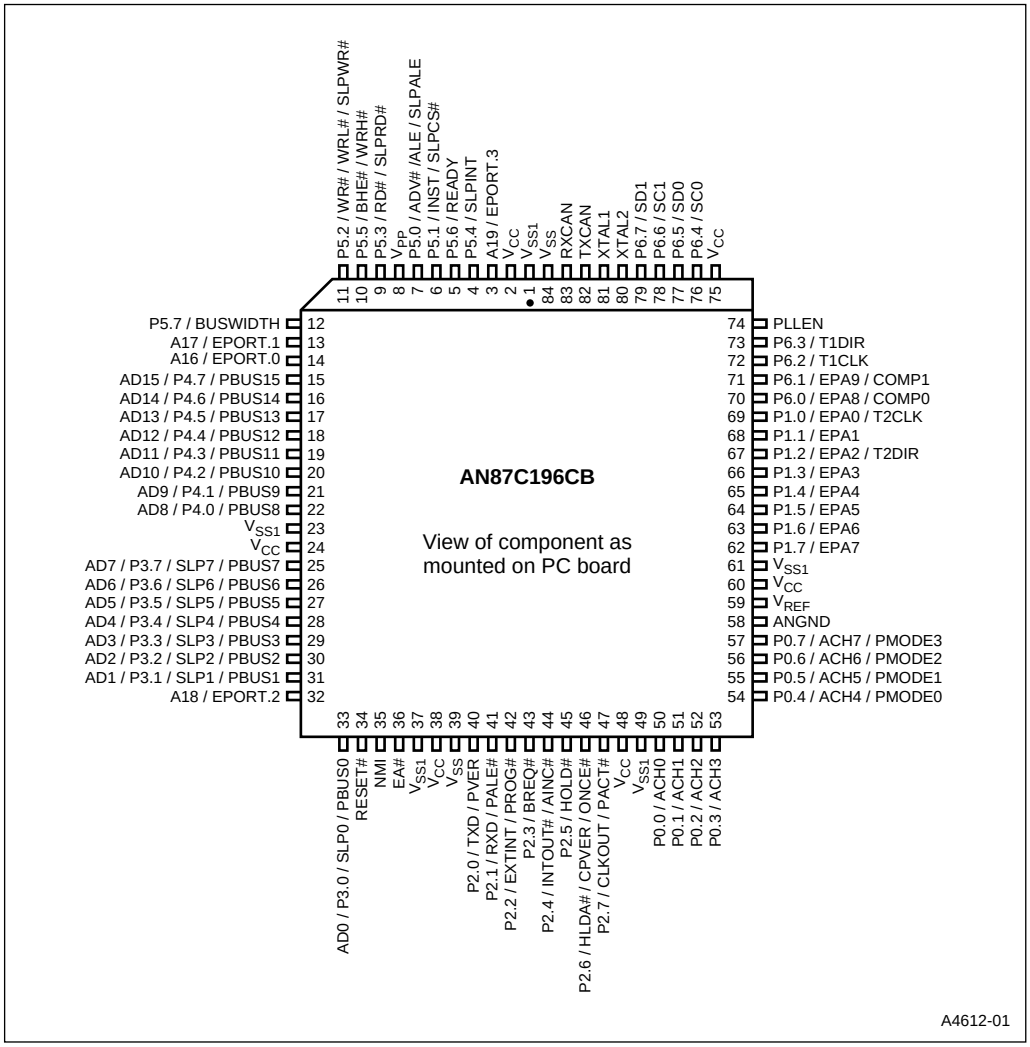


Affected Docs: *87C196CB Supplement to the 8XC196NT User's Manual* - 272787.

3. Appendix A; Signal Descriptions

Issue: Figure A-1. 87C196CB 84-pin PLCC package, pin 39:

- WAS - "V_{SS1}"
- IS - "V_{SS}"



Issue: Figure A-2. Package type:

- WAS - depicted as "87C196CB 100-pin PLCC package"
- IS - depicted as "87C196CB 100-pin QFP package"

Affected Docs: *87C196CB Supplement to the 8XC196NT User's Manual* - 272787.