

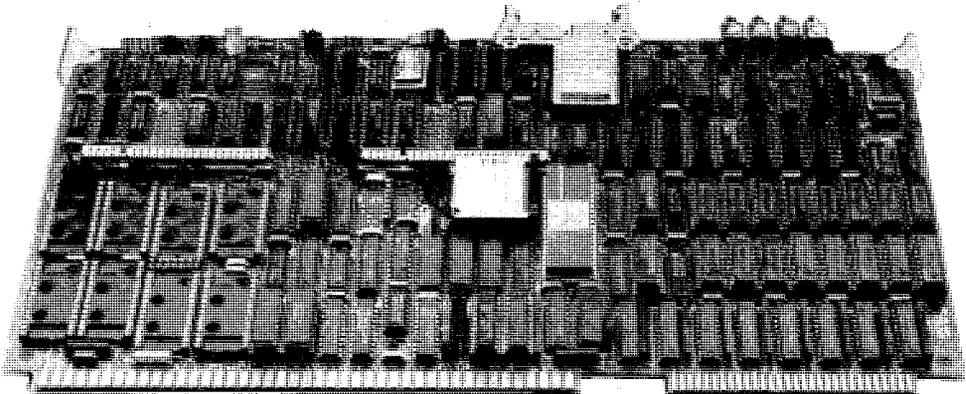


iSBC[®] 186/78A INTELLIGENT VIDEO GRAPHICS CONTROLLER

- 8 MHz 80186 Integrated Microprocessor
- Top Drawing Speeds of 1.25M Pixels/sec
Polygon Drawing Rate: 150K Pixels/sec
- Programmable Frame Rate and Size
- Simultaneous Multiwrite into All Planes
- Two iSBX[™] Bus Connectors
- DMA to Local Bus from iSBX[™]
MULTIMODULE[™], Local Memory, and
MULTIBUS[®] System Bus
- Optional VDI (Virtual Device Interface)
Graphics Software Resides On-Board
- Look-Up Table Generates up to 16 out
of a Possible 4096 Colors
- i82720 Graphic Display Controller
- Resolution of 640 x 480 (Non-
Interlaced) or 1024 x 800 (Interlaced)
- Eight 28-Pin Memory Sites
- Multiple Co-Resident Frame Buffers
- Serial Input Support for Human
Interfaces via iSBX[™] MULTIMODULE[™]
Board
- Full RS-343 or RS-170 Support

The iSBC 186/78A VGC (Video Graphics Controller) is the newest member of Intel's growing family of micro-computer graphics products. It provides an economical, off-the-shelf graphics solution for OEM applications. The local microprocessor (80186) adds on-board intelligence to off-load graphics functions from the host CPU. Powerful bit-mapped graphics are made possible by the Intel 82720 Graphics Display Controller (GDC). This display controller supports high level drawing commands including arcs, circles, rectangles, area filling, zoom, panning and scrolling.

The iSBC 186/78A VGC board functions either as a host CPU with integral graphics, or as a dedicated graphics controller. Graphics applications can communicate directly with the optional on-board VDI (Virtual Device Interface), a standard graphics software interface. Applications that will benefit from the iSBC 186/78A VGC include process control monitoring, automatic test equipment, transaction processing, and instrumentation.



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*UNIX is a trademark of Bell Labs

ARCHITECTURAL OVERVIEW

The iSBC 186/78A integrates both a high performance 80186 microprocessor and a medium resolution graphics display controller on one board, serving both the computational and display requirements of today's interactive applications. The iSBC 186/78A VGC operates with Intel's standard graphics software (iVDI 720), an implementation of the proposed Virtual Device Interface standard.

In the past, MULTIBUS graphics boards combined two functional blocks on a single iSBC board; e.g., graphics control and MULTIBUS interface logic. Now, Intel has integrated a third block; an on-board 80186 microprocessor provides a control center for the local graphics capabilities. In addition, the large display memory area allows multiple buffering of consecutive images for a tremendous improvement in image display performance. Each of these functional areas is highlighted in Figure 1, and detailed in separate sections.

Such high integration results in two significant benefits to the user: (1) increased system performance by off-loading the graphics routines from the host CPU board, and (2) increased savings due to the compact, single board implementation. Distributed graphics processing results in a system cost that is more directly proportional to the number of users serviced, without adversely impacting per-user performance.

In low cost applications, the on-board microprocessor also allows the iSBC 186/78A VGC to function as a host CPU with integral graphics.

GRAPHICS PROCESSOR FUNCTIONS

Graphics Display Controller

The Intel 82720 GDC is an intelligent graphics controller designed to operate as the heart of a raster-scan computer graphics display system. The 82720 GDC performs all the basic timing needed to generate the raster display and manage the display memory. In addition, the 82720 GDC supports several high level graphics figure drawing functions. Table 1 highlights the 82720 command set.

Both the graphics mode and the mixed mode of the 82720 GDC are supported, although the iSBC 186/78A VGC does not use an external character generator. The internal zoom-write feature of the GDC is fully supported. There is no external zoom circuitry. DMA to and from the display memory is supported via the MULTIBUS data bus, the local bus or through the iSBX data bus.

Display Memory

The iSBC 186/78A VGC contains 512K bytes of high-speed display memory, all of which is under the control of the 82720 GDC. The 82720 GDC controls both writing and reading data to and from the display memory and refreshing the screen.

The configuration of on-board display memory may be set under user program control. The display memory may be segmented into multiple frame buffers, for example: three 640 x 480 x 4 frame buffers

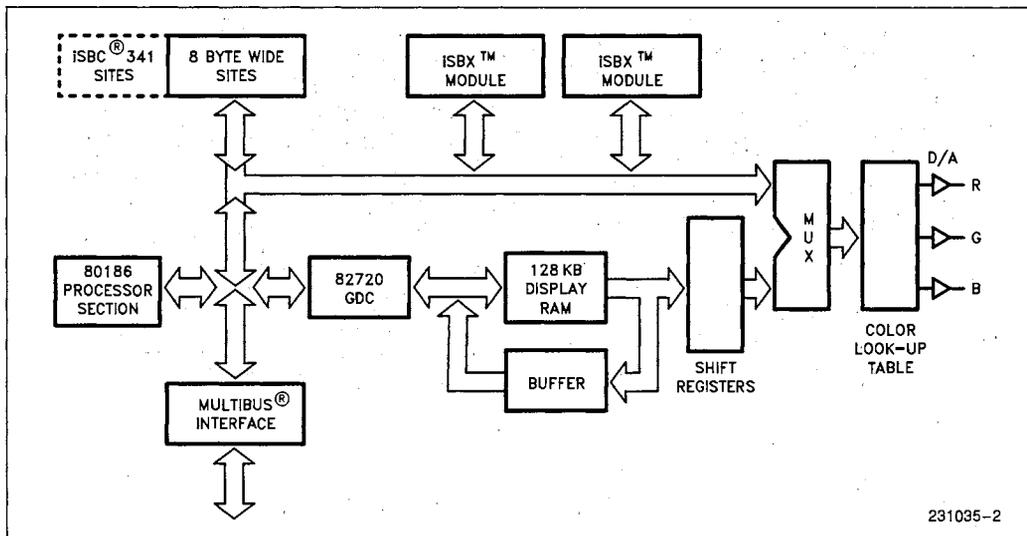


Figure 1. Block Diagram

Table 1. 82720 Command Library

Video Control Commands	
RESET:	Resets the GDC to its idle state.
SYNCH:	Specifies the video display format.
Display Control Commands	
START:	Ends idle mode and unblanks the display.
BCTRL:	Controls the blanking and unblanking of the display.
ZOOM:	Specifies the zoom factors for graphics character writing.
CURS:	Sets the position of the cursor in display memory.
PRAM:	Defines the starting address and lengths of display areas, and specifies the eight bytes for the graphics character.
PITCH:	Specifies the width of the X dimension in display memory.
Drawing Control Commands	
WDAT:	Writes data words or bytes into display memory.
MASK:	Sets the mask register contents.
FIGS:	Specifies the parameters for the drawing processor.
FIGD:	Draws the figure as specified.
GCHRD:	Draws the graphics character into display memory.
Data Read Commands	
RDAT:	Reads data words or bytes from display memory.
CURD:	Reads the cursor position.
LPRD:	Reads the light pen address.

or four 512 x 512 x 4 frame buffers. Display memory is read or written 16 bits at a time by the 82720 GDC. Both display cycles and read-modify-write (RMW) cycles may be controlled by the user. During display cycles, data is read from the display memory and sent to the CRT for display, starting at the upper left hand of the screen and moving down toward the bottom right corner. During RMW cycles, data is transferred between the GDC and the display memory.

In monochrome mode, all 256K 16-bit words are treated as a contiguous block of memory, where a logical "1" in memory is displayed as an illuminated pixel. In color mode, four color planes exist in memory and are written into (multi-write) and displayed simultaneously. Each plane consists of 64K 16-bit words.

Video Output

The iSBC 186/78A VGC controls both monochrome and color monitors, providing TTL (0V–5V) or analog (0V–0.7V) signal outputs. The iSBC 186/78A VGC operates with a broad range of CRT horizontal scan-rates. (The scan-rate is related to the pixel clock rate and the desired display resolution.) The pixel clock rate is selected by a jumper on the board, and may be either 20 MHz or 25 MHz. The pixel clock oscillator may be changed by the user to support monitors with lower bandwidths.

MONOCHROME MONITORS

The iSBC 186/78A VGC video outputs and sync signals may be either TTL or analog level signals. The sync signals are available as separate vertical and horizontal sync signals (Vsync and Hsync) or as a composite sync signal (Csync). When the iSBC 186/78A VGC operates in the monochrome mode, the analog video signal can provide a 16-level grey scale.

COLOR MONITORS

When operating in the color mode, the iSBC 186/78A VGC video outputs are Red, Green, and Blue video signals, with a maximum of 16 individual colors displayed at one time. The Red and Blue output signals are always analog. The Green output signal may be analog or TTL. The analog signals are generated in a 12-bit look-up table that provides a possible 4096 colors. When the Green output is analog, it may be combined with the composite sync signal, producing a Sync-on-Green signal. The vertical and horizontal sync signals (Vsync and Hsync) are available on separate outputs or they may be combined to generate a composite sync signal (Csync).

GRAPHICS CONTROL CENTER

Central Processing Unit

The 80186 component is a high-performance, high-integration 16-bit microprocessor. It combines several of the most common components onto a single chip including DMA (Direct Memory Access), interval timers, clock generator, and a PIC (Programmable Interrupt Controller). The 80186 CPU provides up to a 100% performance improvement over the 8086 CPU at an equivalent clock rate.

Three internal 16-bit programmable timers are provided. On the iSBC 186/78A VGC, two of these flexible timers are connected to four external pins (two pins per timer). They can be used to count or time

external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. User software can configure each timer independently to select the desired function. Available functions include: Interrupt on terminal count, programmable one-shot, rate generator, square-wave generator, software triggered strobe, hardware triggered strobe, and event counter. In addition, the third timer can be used as a prescaler for the other two timers, or as a DMA request source. The contents of each counter may be read at any time during system operation.

A 6-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 500 ns minimum instruction cycle to 333 ns for queued instructions. The stack oriented architecture readily supports modular programming by facilitating fast, simple intermodule communication along with other programming constructs needed for asynchronous real-time systems.

The 80186 CPU uses a dynamic relocation scheme that allows separation of command procedures from data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K bytes at a time. Activation of a specific register is controlled, both explicitly by program control, and implicitly by specific functions and instructions. In addition, the iSBC 186/78A VGC has external logic to provide access to the full 16M byte range of the MULTIBUS address space.

Both DMA channels provided by the 80186 CPU are supported on the iSBC 186/78A VGC. These channels allow a direct path from the MULTIBUS or iSBX bus to local memory. Indirect access to the display memory is also possible under 82720 GDC control.

A flag byte signaling mechanism aids in creating an interprocessor communication scheme. This includes: (1) the ability to set/reset interrupts and (2) board reset.

Instruction Set

The 80186 instruction library is a superset of that for the 8086. Therefore, object code compatibility was maintained while 10 instructions were added. The new instructions include: Block I/O, Enter and Leave subroutines, Push Immediate, Multiply Quick, Array Bounds Checking, Shift and Rotate by Immediate, and Pop and Push All.

Universal Memory Sites for Local Memory

Eight 28-pin JEDEC-compatible sockets are provided for using 2732, 2764, 27128, 27256 and 27512 EPROMs and their respective ROMs. Other JEDEC-standard pinout devices are also supported, including byte-wide static RAMs and iRAMs. Expansion to a total of 12 sockets is available by adding the iSBC 341 memory module. With the iSBC 341 memory module installed, the board supports up to 768K bytes of local storage (using 27512 EPROMs).

The eight sockets are divided into four blocks of two each (for high and low byte), or six blocks when using the iSBC 341 memory module. These independent blocks allow the user to mix many different kinds of 28-pin devices for increased application flexibility. Two different kinds of components may be used at any one time and all devices on the optional iSBC 341 memory module must be the same. The memory decode PAL is socketed so that the user may replace it with a custom PAL configured to suit their particular application.

Interrupt Control

The iSBC 186/78A VGC board uses the programmable interrupt controller (PIC) within the 80186 component, and allows 5 on-board vectored interrupt levels. The highest priority interrupt is the Non-Maskable Interrupt (NMI) line which is tied directly to the 80186 CPU. This interrupt is typically used to signal catastrophic events (e.g. power failure). The PIC provides prioritization and vectoring for the other 4 interrupt requests from on-board I/O resources and from the MULTIBUS system bus. The PIC then resolves the requests according to the programmable priority resolution mode, and if appropriate, issues an interrupt to the CPU.

Interrupt service requests to the iSBC 186/78A VGC may originate from 22 sources. Table 2 contains a list of devices and functions capable of generating interrupts. Most of these interrupts may be jumpered (user configurable) to the desired interrupt request level.

iSBX™ MULTIMODULE™ Expansion

The iSBC 186/78A VGC has two iSBX MULTIMODULE connectors, both support the 8-bit and 16-bit iSBX data buses. The addition of iSBX MULTIMODULE boards provides I/O functions to suit most application requirements. These I/O functions can in-

Table 2. Interrupt Request Sources

Device	Function	Number Interrupts
MULTIBUS interface INT0-INT7	Requests from resident MULTIBUS CPU or peripheral controller boards	8
Internal 80186 timer and DMA	Timer 0, 1, 2, outputs (function determined by timer mode) and 2 DMA channel interrupts	5
iSBX interfaces	Function determined by iSBX MULTIMODULE boards	6
Bus fail-safe timer	Indicates addressed resident MULTIBUS device has not responded to command within 6 msec	1
GDC vertical retrace	Synchronization of screen blanking	1
Flag Byte	Board identification	1

clude parallel and serial I/O, analog I/O, and mass storage device control. Mounting iSBX MULTIMODULEs directly on the single board computer often results in less interface logic, lower power, simpler packaging, higher performance, and lower costs than an alternative full-size iSBC board solution. See Figure 2 for an example of a minimal system where iSBX MULTIMODULE boards are added to an iSBC 186/78A VGC acting as the host CPU.

Each of the iSBX connectors on the iSBC 186/78A VGC provides all of the signals necessary to interface to the local on-board bus, including 16 data lines for maximum data transfer rates. All iSBX MULTIMODULE boards, designed with 8-bit data paths and using the 8-bit iSBX connector, are also supported on the iSBC 186/78A VGC. A broad range of iSBX MULTIMODULE options are available from Intel.

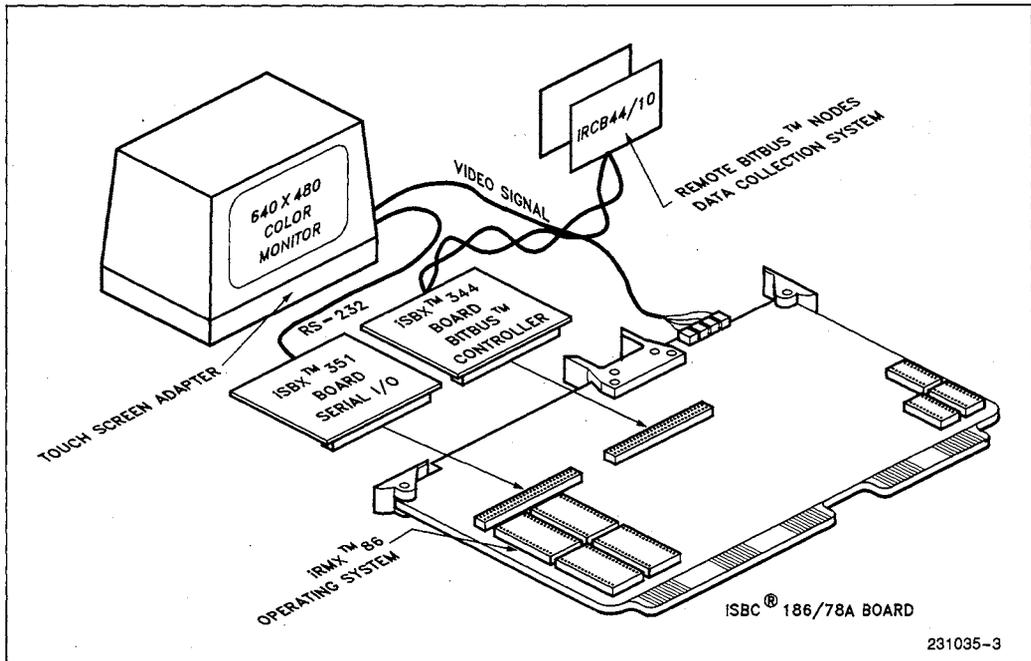


Figure 2. iSBC® 186/78A as a Host-CPU

MULTIBUS® SYSTEM ARCHITECTURE

System Bus—Overview

The MULTIBUS system bus is Intel's industry standard (IEEE 796) microcomputer bus structure. Both 8-bit and 16-bit single board computers are supported with 24 address and 16 data lines. A MULTIBUS system can be expanded by using a variety of MULTIBUS board products, such as the iSBC 186/78A VGC. The bus structure also allows very powerful distributed processing configurations with multiple processors, including multiple iSBC 186/78A VGC boards, for the most demanding microcomputer applications.

Multimaster Capabilities

For those applications requiring additional processing capacity and the benefits of multiprocessing (i.e. several CPUs and/or controllers logically sharing system tasks), the iSBC 186/78A VGC provides full MULTIBUS bus arbitration control logic. This control logic allows up to three iSBC 186/78A VGCs, or oth-

er bus masters, to share the system bus using a serial (daisy chain) priority scheme. Up to 16 bus-masters may share the MULTIBUS system bus with an external parallel priority decoder. In addition to the multiprocessing configurations made possible with multimaster capability, the MULTIBUS system bus also provides an efficient mechanism for all forms of DMA (Direct Memory Access) transfers. Figure 3 shows a multiuser, multimaster configuration.

MULTIBUS® Expansion

Memory and I/O capacity may be increased and additional functions added by using Intel MULTIBUS compatible expansion boards. System memory for the 80186 microprocessor may be expanded by adding RAM boards, EPROM boards, or memory combination boards. Digital I/O and analog I/O expansion boards are available. Floppy disk and hard-disk controllers are available on MULTIBUS expansion boards or iSBX MULTIMODULE boards. Modular, expandable backplanes and cardcages are available to support multi-board systems.

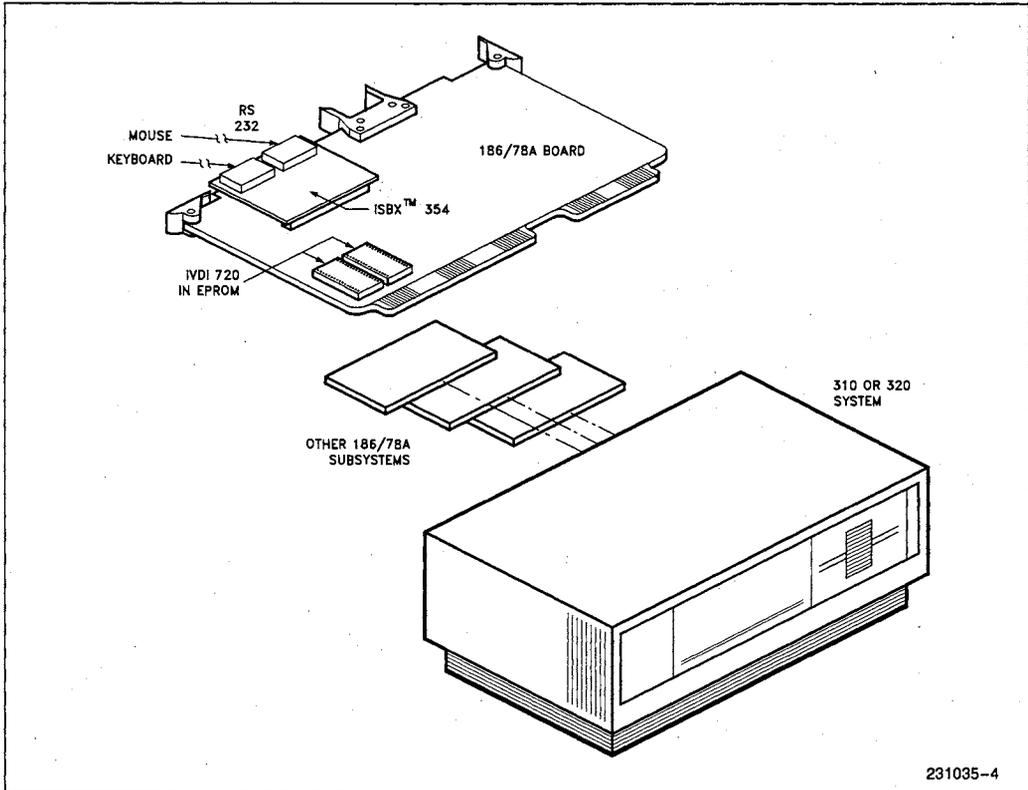


Figure 3.

GRAPHICS SOFTWARE (OPTIONAL)

iVDI 720 Command Interpreter

The iVDI 720 Virtual Device Interpreter provides the iSBC 186/78A VGC with a Virtual Device Interface (VDI) that is consistent with the graphics software standard defined by the ANSI X3 organization. The iVDI 720 software decodes high-level commands to streamline the development of application code. It also supports a variety of input device drivers including digitizing tablets and mice. The standard software interface provides a smooth upgrade path, simplifying the transition to future hardware devices.

The proposed ANSI standard defines the encoding of high-level text and graphics commands. The iVDI 720 software decodes a binary representation of these proposed commands, and allows consistent formatting and storage of VDI encoded images.

The iVDI 720 Graphics Virtual Device Interpreter is designed for EPROM installation on the iSBC 186/78A VGC. Graphics functions can then be off-loaded to the iSBC 186/78A VGC, permitting the host CPU board to concentrate on system level operations such as database management or network communications.

iRMX™ 86/iRMX 286 Software Device Driver

The iRMX 86 and iRMX 286 software are Intel's real-time, multi-tasking operating systems. The iVDI 720 software package furnishes the software device driver required to operate the board in an iRMX software environment. It creates a predictable environment for the input and output of high-level commands between the user and system, or among the graphics peripherals attached to the system, such as a mouse, tablet, printer or plotter. The iRMX driver includes PL/M and C language bindings.

SPECIFICATIONS

Word Size

Instruction—8, 16, 24, or 32 bits

Data —8 or 16 bits

System Clock

8.00 MHz \pm 0.1%

Instruction Cycle Time

8 MHz —500 ns

—333 ns (assumes instruction in queue)

NOTE:

Basic instruction is defined as the fastest instruction time (i.e., two clock cycles).

Memory Response Time

286 ns for zero wait-states (address to data-valid)

Memory Capacity (Max)

EPROM 512K bytes (768K with iSBC 341 MULTIMODULE) using 27512s

E²PROM 16K bytes (24K with iSBC 341 MULTIMODULE) using 2817As

iRAM 64K bytes (96K with iSBC 341 MULTIMODULE) using 51C86s

Static RAM same as iRAM

PHYSICAL CHARACTERISTICS

Length: 12.00 in. (30.48 cm)

Height: 7.05 in (17.90 cm)

Depth: 0.50 in. (1.78 cm)

1.13 in. (2.82 cm) with iSBC Memory Expansion and MULTIMODULEs, or iSBX MULTIMODULE boards

Weight: 18.3 ounces (519 gm) excluding any MULTIMODULE boards



Connectors

Interface	Double-sided	Centers	Supplier
MULTIBUS System	86 pin (P1)	0.156 in.	Viking 3KH43/9AMK12 Wire Wrap
iSBX Bus (8- and 16-bit)	36/44 (J2, J3)	0.100	Viking 000294-0001
Video Interface - or -	26 (J1) 5 pcs. (J7-11)	0.1 SMC-type	3M 3399-6026 flat cable Sealectro 50-007-0000, with Belden 174/U coax

ELECTRICAL CHARACTERISTICS

Power Requirements: 8.4A @ +5 ± 5% Vdc (Maximum); 4.9A @ +5 ± 5% Vdc (typical)

ENVIRONMENTAL REQUIREMENTS

Operating Temperature: 0° to 55°C with 200 lfm air flow

Relative Humidity: to 90% without condensation

REFERENCE MANUAL

147393-001— iSBC 186/78A Video Graphics Subsystem Hardware Reference Manual

RELATED LITERATURE

- 210883-001— MULTIBUS Handbook
- 280002-001— iVDI 720 Data Sheet (Virtual Device Interface)
- 146717-002— iVDI 720 Graphics Software Reference Manual
- 142686-001— iSBX Specification
- 210451-001— 80186 Data Sheet
- 210655-001— Intel 82720 Data Sheet

Literature and Hardware Reference Manual may be ordered from an Intel Sales Representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
iSBC 186/78A	Intelligent Video Graphics Subsystem